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APPLICATION OF DIGITAL CONTROL TO A MAGNETIC MODEL SUSPENSION AND BALANCE MODEL

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PREFACE

This Final Report covers work performed on NASA Grant NSG 1292 between April 1, 1976 and November 30, 1977 under the Technical Cognizance of Mr. Richmond P. Boyden, Subsonic-Transonic Aerodynamics Division, NASA-Langley Research Center.

The use of trade names in this paper is essential to a proper understanding of the subject material; their use in no way implies endorsement.

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To convert from inches to meters, multiply by 0.0254

Chapter I

INTRODUCTION

Since the advent of a systematic procedure for designing automatic control systems a generation ago, automatic control systems are becoming more common. At this time one can foresee an evolutionary step whose importance is comparable with that of a generation ago. This important step is the introduction of digital computers to replace analog computing elements in these systems. With the advancement of digital technology, digital computers have continuously become more efficient, expanding into new applications with each major technological improvement. Recently the power of digital computers has been made available at the integrated circuit level. They compute very fast, and are multifunctional, small and reliable. They give rise to the possibility of using dedicated digital processing units for a variety of complicated tasks; for example, the inclusion of digital processors as parts of various process control systems.

This report presents the results of a study which indicates that replacing the analogue control system for the MIT-NASA prototype magnetic balance with a digital system is feasible. Preliminary tests with a one-dimensional suspension system were successful and it appears that a digital control system can greatly improve the speed, accuracy and versatility of magnetic balance operation.

Magnetic balance and suspension systems for wind tunnels have been in use for over a decade (1,2) and have proved useful not only because of their accuracy but also because they offer the opportunity to conduct classes of tests that have been difficult to carry out in the past.

The basic idea of the MMSB can be explained using the functional block diagram in Figure 1. As it is shown, the suspension system is a position control servo, designed to maintain the suspended model at some set position within the suspension magnet structure, according to the position command signals. The position of the model is translated into electrical signals by means of a position sensing device, and these signals are compared with the position command signals. The resulting position error signals are modified in passing through a set of feedback compensation networks.

The compensated error signals are then amplified and applied to the suspension system magnet coils. The magnetic fields produce magnetic forces on the suspended model according to the "magnetic force and moment relations" which are functions of the model position and orientation, as indicated by the internal feedback path. The magnetic forces and moments added to the aerodynamic and gravity forces and moment, act through the model inertias to cause changes in the position and orientation of the model. These changes are in turn sensed by the position sensor system and the servo loop is closed. The function of the servo loop is to minimize the integral of position error by continuously counteracting the aerodynamic and gravity loads.

In addition to maintaining model position it is necessary to determine the aerodynamic loads acting on the suspended model. As we can see, the unknown aerodynamic forces and moments applied to the model by the wind are balanced against gravitational forces and moments, and magnetic forces and moments. Since gravitational forces and moments are known, the magnetic forces and moments can be calculated from electrical currents flowing through the magnetic coils and appropriate calibrations. As a result the aerodynamic forces and moments are determined within the limits of experimental accuracy.

The following sections of the report describe:

1. The present analog control MMSB system at the M.I.T. Aerophysics Laboratory.

2. Experimental measurements and design studies of the continuous analog control MMSB system.

3. Sampled-data analysis for digital control of lift and pitch axes.

4. Hybrid simulation by using PDP 11/10 digital computer for control and an analog computer to simulate the magnetic coils and model.

5. Description of the microcomputer.

6. Real time digital control of the one-dimensional magnetic balance.

7. Estimation of the attainable limits of accuracy of model location and attitude.

8. Conclusions and recommendations.

Chapter II

DESCRIPTION OF MIT-NASA MAGNETIC MODEL SUSPENSION AND BALANCE SYSTEM

Background

MIT-NASA magnetic suspension and balance system at the Aerophysics Laboratory has five controllable degrees of freedom for ferromagnetic wind tunnel models: lift, drag, slip, pitch and yaw. The model can also be rotated at variable speed.

Development of magnetic suspension and balance systems for wind tunnels was begun at M.I.T. in 1957, shortly after publication of the work of Tournier and Laurenceau (3). Chrisinger (1), Tilton and Schwartz (4) and Tilton and Baron (5) were responsible for the initial work on the problem done at M.I.T.

Work on the MIT-NASA magnetic suspension and balance system began in 1963 under NASA-Langley Research Center Contract NASA-4421. It was in late 1969 that the initial checkout was complete (6).

The present MMSB system consists of the following subsystems: a magnet coil assembly, a model position sensor system, a compensation system and a power amplifier system. The magnetic coil assembly generates the necessary magnetic field. Model position sensors sense the position of the model. Compensators provide the automatic control of the system. Power amplifiers amplify the compensated error signals to drive the magnetic coil assembly.

The position sensing device (6), Electromagnetic Position Sensor (EPS), is basically a multi-component differential transformer with the model forming the core. A simplified schematic is shown in Figure 2 and the prototype EPS system transducer coil assembly is shown in Figure 3. The excitation windings are powered by a constant voltage amplifier at 20 KHz. Movement of the model varies the coupling between the excitation windings and the pickup windings. The pickup coil voltages are then processed, including filtering, amplifying, summing and demodulating, to give high level outputs which are approximately proportional to the displacements of the model relative to the axes of the transducer assembly.

A functional block diagram of the MIT-NASA MMSB system is presented in Figure 1. Several assumptions were used in the design of the present continuous compensation system (6).

1. Each degree of freedom is uncoupled from the others. That is to say, we can treat them as uncoupled channels and design and analyze them independently.

2. The transfer function from power amplifier input signal to the magnetic coil current is characterized by a first order lag.

3. Magnetic force is assumed to be proportional to and in phase with the magnet current.

4. The measured model position is assumed to be proportional to and in phase with the actual model position.

The first assumption is approximately valid for the MIT-NASA MMSB for small angles of attack, and is assumed again in the preliminary design of the sampled-data control system. All other assumptions are made again for the purposes of this chapter and will be discussed at its end.

A good compensator should accomplish three things:

1. Stabilization of the loop.

2. Minimization of the integral static position error for given force disturbance inputs.

3. Minimization of the integral static position error for given position command inputs.

Consider the translational components (lift, drag and slip) first. They are essentially similar, characterized by the same form of system equations, with different coefficients. One channel is shown in simplified form in Figure 4. In order for the compensator to be quite simple and effective for a wide range of models and angles of attack, the form in Figure 5 is adopted. It consists of three paths: proportional, integral and third-order lead-lag network. The integrator is included to maintain zero position error at steady force input.

The servo-loop diagram for this configuration is shown in Figure 6. In the plot there are five circled numbers. They indicate the points at which data were taken. (This procedure will be explained in the next chapter.) With

appropriate combinations of gains and settings of poles and zeros of the compensator, satisfactory operation is achieved for a wide range of conditions. Root loci of lift and drag axes for a copper plated ellipsoidal core under certain combinations are given in the next chapter.

The pitch and yaw axes are slightly different from the translational components, the main difference being the angular response to moment inputs. The model thus appears held by a torsional spring having natural frequencies determined by the magnetic and inertial properties of the model (2). This has the effect of separating the model dynamic poles symmetrically from the origin, as will be shown in the root locus diagram of the next chapter.

Another point is that the pitch and yaw position signals are supplemented by two laser angle-sensing elements. These elements supply the integral loops of the control systems holding the model at a set angular position. The laser integrators were not used during the tests described below.

Measured Performance of the Original Analogue System

In order to have confidence in the analytical design of the digital system, the static and dynamic performance characteristics of the continuous analogue components were measured experimentally. The experiment included:

1. Static calibration of the Electromagnetic Position Sensor system for lift, drag, pitch and yaw degrees of freedom.

2. Dynamic performance of the lift, drag and pitch degrees of freedom.

The model used was the copper plated ellipsoidal core, as shown in Figure 7. Static position outputs of the EPS were calibrated with the aid of a set of transits. All static data were fed into a Hewlett Packard 2401C integrating digital voltmeter and recorded on a HP J66562A digital recorder. Dynamic data were recorded on a Sanborn 4500 series recorder and were monitored on oscilloscopes.

In this chapter these experiments and the data reduction procedure will be described. Analytic models of the MMSB system will then be presented and compared to the experimental data.

A. Static Calibration of the Electromagnetic Position Sensor System

Calibrations of the EPS output versus model position were made for the lift, drag, pitch and yaw degrees of freedom. Relations between output and position are linear, and there is some coupling among axes, as will be described below.

The model was suspended at the center of the tunnel and then repositioned in one direction only (i.e., pure lift, pure drag and so forth) at several different distances. The relative displacement to the center of the tunnel was measured with the aid of a set of transits. Output of this axis as well as all other axes were recorded. Using the mathematical linear regression method, we have equations in the form $y = ax + b$; i.e., EPS output in millivolts (y) versus displacement (x). The results of the calibration could be summarized by a single matrix equation, $y = ax + b$, as given in Equation 2.1.

$$\begin{bmatrix} L \\ D \\ P \\ Y \end{bmatrix} = \begin{bmatrix} 337.2 & 0 & 0.59 & 0 \\ 0 & 540.5 & 4.6 & 0 \\ 17.5 & 0 & 16.4 & 0.72 \\ 0 & -75.5 & -1.45 & 27.8 \end{bmatrix} \begin{bmatrix} L(\text{inch}) \\ D(\text{inch}) \\ P(\text{degree}) \\ Y(\text{degree}) \end{bmatrix} + \begin{bmatrix} -38.5 \\ -4.7 \\ 90.3 \\ 57.7 \end{bmatrix}$$

EPS Output in mV — Model Displacement — Offset in mV

2.1

The diagonal elements of the matrix A are static sensitivities of the EPS caused by model movements. All off-diagonal elements of the matrix are caused by the coupling between axes, and are much smaller than the corresponding diagonal elements. All channels also have offset voltages.

As a matter of test procedure, the diagonal values have been checked each time the suspension has been subsequently used, and the values have remained within five per cent of the listed values during the entire testing period. However, the sensitivity is known to be somewhat dependent upon the relative humidity.

B. Dynamic Performance

In order to obtain transfer functions of the continuous components of the system, the frequency response of the closed-loop continuous system was measured. We followed the assumption that each channel was essentially uncoupled, and could be treated independently. For the purpose of this design study we excluded the integrator as part of the compensator for lift and pitch axes, but included it for the drag axis, as will be explained at the end of this chapter.

The copper plated ellipsoidal core was first suspended at the center of the tunnel under a certain combination of settings of gains and poles and zeros of the compensator. A sinusoidal input perturbation was then added as the position command signal, with frequency range from 0.04 Hz up to about 20 Hz. Signals at five different points were measured, as shown in Figure 6. These signals were recorded on a Sanborn recorder.

By measuring the voltages at these points the individual Bode magnitude and phase plots of each component were obtained. These data were then approximated by transfer functions to the extent possible. The resulting block diagrams are given in Figures 8, 12 and 17 for the lift, pitch and drag degrees of freedom. In these diagrams the transfer function of each component is normalized to its corresponding D.C. gain and the overall feed forward and feedback gains are put in separate blocks for convenience. The open loop frequency response is given in Figures 9, 13 and 18. For these plots the experimental data points are shown by dots, and the solid curves are the analytical results obtained using the assumed transfer function. The low frequency data permitted us to estimate the open-loop static gain.

In addition to the frequency response correlation for each component the transfer function data was used to predict the closed-loop characteristics. The root locus diagrams were obtained, as shown in Figures 10, 14, 15 and 19. For the estimated open-loop static gains the closed-loop Bode plots were obtained, as shown in Figures 11, 16 and 20 for the lift, pitch and drag degrees of freedom, respectively.

The correlation between theory and experiment is adequate for system design. Several comments are in order:

1. As mentioned at the beginning of the Dynamic Performance Test, these experiments were done for a certain combination of settings of gains and poles and zeros of the compensator for the copper plated ellipsoidal core. This means only that this compensation was workable; i.e., the model could be suspended with

reasonable characteristics. It does not mean the combination was the best. If we had changed the combination or changed the model, the data would have been changed. However, the closed-loop tests verified that the analytical modeling of the analog components was sufficiently adequate, and that was the point of this design study.

2. The integrator is included in the compensator in order to maintain zero position error at steady disturbance input, and it is in parallel with two other paths. If the integrator gain Ki is comparable with 1, the effect of the integrator is only present at very low frequency. Because of this the integrators were excluded from the compensators for the lift and pitch degrees of freedom in this study to simplify data analysis for the other parts of the system. As we shall see in the next chapter, there will be no difficulty in adding an integrator to the sampled-data control system.

3. These results are valid only for small displacements. The reason is that the suspension characteristics vary with model position, resulting in a non-linear system. This indicates that many things can be done in the future in the non-linear control area to increase the range of operation.

4. As mentioned above several assumptions made in the original design have been modified by the above experiment. Specifically we obtained:

a. An explicit representation of the power amplifiers which are characterized by second-order lags.

b. An explicit representation of the transfer functions from magnetic field currents to the EPS outputs. For the lift and drag degree of freedom these are approximated by second-order integrators. For the pitch axis, there are a pair of complex poles with one real zero. These complex poles are the result of the spring effect mentioned above. The reason that they are not on the imaginary axis is believed due to eddy current losses in the model (7).

Chapter III

DESIGN OF SAMPLED DATA CONTROL FOR LIFT-AND-PITCH AXES

The first requirement of a digital control system for the MMSB is to provide for automatic control. Since models are required to perform coning motion up to 15 Hz, the resultant system should have a good frequency response in pitch and yaw axes up to 15 Hz.

The block diagram for the lift degree of freedom is shown in Figure 21. In the plot the analog system includes the power amplifier, magnetic coil, model and Electromagnetic Position Sensor. The digital system includes a digital filter in the feedback path and an integrator in parallel with the proportional signal in the feed forward path. The position signal from the EPS is sampled at the sampling frequency and fed to the digital filter which is put in the feedback path to reduce overshoot. The position command signal is sampled at the same rate, and added to the output of the digital filter. The sum is then passed through the parallel path, including proportional and integral components, to maintain zero position error at steady disturbance input. The resultant signal is fed to a digital-to-analog convertor and sample-and-hold circuit, and then fed to the analog system.

From Figure 11 the closed-loop cutoff frequency of the lift axis for the present continuous control system is about 40 radians per second (6.4 Hz). The input frequency will not exceed 15 Hz. The sampling frequency selected was 33.3 Hz with a sampling period of 0.03 second. This was chosen such that there was no aliasing, but was otherwise arbitrary.

The second step was to get a discrete representation of the analog system, including the zero order hold circuit. This was done by taking the Z transform of the analog part, where $Z = e^{TS}$, T = sampling period. We then specified the desired performance capability in terms of the natural frequency, damping ratio and zero locations of a continuous second order system, which was called the MODEL. The idea of constructing a MODEL is that one could optimize the closed loop response of the lift degree of freedom so as to approximate that of the MODEL. The MODEL used had a pair of complex poles at $0.7 \pm 0.3j$ and a single zero at the origin in the Z plane.

The integrator gain K_i was then selected based on the desired low frequency response when the model was subject to disturbance input. $K_i = 0.5$ was chosen with response time

about five seconds with respect to disturbance input. We then compensated the system using a digital filter to get the desired performance. A second order digital filter was selected for the lift axis. Using root locus technique, one then had a first estimate of the possible coefficients of the filter and the corresponding static open loop sensitivity. The selected coefficients were only a first guess. To refine the compensation characteristics, parameter optimization techniques were used. The parameter optimization technique used here was developed for the design of linear automatic control systems applicable to both continuous and digital systems (8). In these techniques the Model Performance Index is used as the optimization criterion because of the physical insight that can be attached to it. The design emphasis is to start with the simplest system configuration that experience indicates would be practical. Design parameters are specified, and a digital computer program is used to select that set of parameter values which minimizes the performance index. The resulting design is examined and complexity, through the use of more complex information processing or more feedback paths, is added only if the performance fails to meet operational specifications. System performance specifications are assumed to be such that the desired step function time response of the system can be inferred.

Using the coefficients obtained from the root locus method as a first guess, and running the parameter optimization program to select the parameters of the second order digital filter, the system of Figure 22 was obtained. The Z-plane root locus for the system is shown together with the step response in Figure 23. The stability boundary in the Z-plane is the unit circle. The system is stable up to an open-loop gain of 280 sec^{-2}. (The gain value is the open-loop gain with the integral compensator path open.) The integrator gain ratio was 0.5.

The design procedure for the pitch axis is similar except that

1. The compensated system should have a good closed-loop frequency response up to 15 Hz. As the result, 33.3 Hz sampling frequency was not fast enough. A new sampling rate of 100 Hz with sampling period 0.01 second was then chosen.

2. The transfer function of the model has one pair of complex poles and one real zero, which result from the spring effect as explained earlier. The closed-loop uncompensated system has very low damping ratio.

This system is shown in Figure 24. The Z-plane root locus for the system together with the step response is shown in Figure 25.

Chapter IV

HYBRID SIMULATION

The preliminary designs of the lift and pitch degrees of freedom were simulated using a hybrid digital/analog computer and step responses of the hybrid systems were measured (10). The digital computer used was the Aeronautics and Astronautics Department's PDP 11/10. The analog computer was TR-48 of Electronic Associates, Inc. The hybrid simulation program was written in BASIC and is listed in Appendix D.

Upon entering the program the difference equation of the digital filter was first calculated from the assigned complex poles and zeros. With a given sampling period and an integrator gain the digital computer could sample the position and position command signals at the sampling rate and calculate a compensated position error signal. The resultant was then fed through an analog-to-digital convertor and zero-order hold circuit to the analog computer.

The program was run on the PDP 11/10 for one degree of freedom at a time. Since the time required for one sample calculation was longer than the sampling period of the designed compensator, the analog system was slowed down to match the PDP 11/10. A time factor of 5 was chosen for the lift degree of freedom, and 10 for pitch axis. (Designed sampling period was 0.03 second and 0.01 second, respectively.)

For the lift degree of freedom the analog computer system is shown in Figure 26. With the designed digital filter, step responses for several combinations of open loop sensitivity K and integrator gain K_i were measured, as listed in Table 1. Percentage overshoot and damped frequency were also calculated. Estimating the dominant mode characteristics gave the results superimposed on the root locus plot of Figure 23, as shown by the heavy dots. The step response for $K = 150$, and $K_i = 0.5$ is given in Figure 27. The time response to a step disturbance force applied to the model is shown in Figure 28. In these plots the time scale has been corrected to read actual records. The pitch axis is similar to the lift degree of freedom. The analog computer diagram is given in Figure 29. Time responses for $K = 16$ and 32 are given in Figure 30.

Two comments are pertinent about the hybrid simulation procedure:

Table 1

RESULT OF LIFT AXIS HYBRID SIMULATION

No.	S_i	S_{01}	Overshoot %	Damped Frequency (rad)
1	0.5	125	21.0	13.1
2	0.5	150	15.0	15.7
3	0.5	200	9.7	33.1
4	0.5	280		36.1
5	1.0	150	18.7	17.5
6	3.0	150	26.7	18.5
7	0	150	13.3	15.7

1. Speed

Some effort was made to write the program in Assembly language, which was believed to be much faster than the program written in BASIC. It was not completed before the microcomputer became available. The Intel 8080 microprocessor with a machine cycle speed of 500 nanoseconds could accommodate the program in BASIC (9). Peripherals of the microcomputer system included analog-to-digital convertor, digital-to-analog convertor and a teletype. Software facilities included a loader, dumper and other basic programs which were stored in programmable read-only memory. This microcomputer was assembled from stock parts of a term project and was returned to stock after completion of the experiments described in this report. It is described in detail in the next chapter.

2. Noise

Most noise was generated by the analog-to-digital convertors. This could be shown by fixing the analog input voltage and printing out the corresponding digital signals, which were noisy.

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Chapter V

DESCRIPTION OF THE MICROCOMPUTER

The prototype microcomputer was based on an Intel 8080 microprocessor and was assembled from components on loan from the M.I.T. Digital Systems Laboratory.* The computer shown in the block diagram of Figure 31 includes three major parts:

Computer body

a. CPU Module

1) Intel 8080 microprocessor
2) Intel 8224 clock generator
3) Intel 8228 system controller
4) Auxiliary controller

b. Memory

1) 2K programmable read-only-memory
2) 1K random-access-memory

c. Input/Output and console

1) Intel 8255 programmable peripheral interface
2) Auxiliary I/O
3) Interrupt handling circuit
4) Front panel

2. Peripherals

a. Teletype and Teletype interface

b. Eight bit A/D convertor with four-to-one analog multiplexer

c. Nine bit D/A convertor with two sample-and-hold circuits

d. Clock

e. Eight channel digital input

*Construction of this microcomputer was carried out by Mr. Luh as part of Course 16.60 in the Electrical Engineering Department under Professor Hoo-Min Toong.

3. Software library

   a. Console monitor

   b. Peripheral service routines

   c. Loader and dumper

   d. Arithmetic routines

   e. Control programs

Throughout this section three number systems will be used; hexdecimal, binary and decimal. So as not to clutter all numbers with subscripted bases, the following general convention will be used:

Hexdecimal: for address locations, contents of addresses and operation codes for instructions.

Binary: for describing a single binary element.

Decimal: for all normal referencing to quantities.

A conversion table is given in Table 2.

2's complement subtractions are used by the 8080 machine.

Table 2

EQUIVALENT NUMBERS

Decimal	Binary	Hexdecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

The basic time cycle of the microcomputer (period of each state) is 500 nanoseconds.

The components shown in Figure 31 are mounted on 22 cards which are inserted into the slots of a portable box. Connections among the cards are made by wires at the back of the slots or through cables which connect different cards. The structure of the computer was limited by the components that were available. In order to avoid lengthy explanation about the theory and operation of the microprocessor itself, Reference 9 is recommended for those who are interested in the detailed circuits. (See Appendix A for Instruction List)

Computer Body

The structure of the computer body follows mostly the design done by Jon Valvano and Randy Haagens of the Digital Systems Laboratory, M.I.T. The schematic is given in Figure 32.

1. CPU Module

CPU module consists of an Intel 8080 microprocessor, an 8224 clock generator, an 8228 system controller, and an auxiliary controller. The auxiliary controller consists essentially of 74174 flip-flops, and is used to latch the status information and generate RDYIN signal for the 8224.

2. Memory

The prototype microcomputer has 2K programmable-read-only memory (1702) with locations from 0000 to 07FF; 1K random-access-memory (2102) with locations from 0800 to 0BFF. Current memory location is decoded from the 16 bit address bus.

Input and output of the memory are connected directly to the 8 bit, tristate data bus. Memory size could be expanded to 64K with some modification of the decoding circuit.

3. Input/Output and Console

This essentially consists of two digital I/O devices, an interrupt handling circuit, and a front panel. The computer body has two digital I/O devices:

a. Programmable peripheral interface. This is the Intel 8255. It has twenty-four pins which are individually programmed in three groups of eight bit each for input or output. The three groups are named port A,B,C respectively.

b. Auxiliary I/O. This is an eight bit bistable latch (two of 7475), and is used for output only.

Both devices connect directly to the tristate data bus. The interrupt handling circuit could handle two interrupts which are caused by two push-buttons on the front panel to perform several different front panel operations.

The front panel includes twenty LEDS, four 7-segment displays, twelve toggle switches (higher eight are DATA SWITCHES, and lower four are FUNCTION SWITCHES), and four push-buttons, as shown in Figure 33. Front panel operations are very much like those of a traditional PDP 11 computer. They include:

Reset	Reset the whole system
Load address	Load high byte of the address Load low byte of the address
Deposit	Deposit a constant to the present address Decrease the address by one and deposit a constant Increase the address by one and deposit a constant
Examine	Examine the content of the present address Decrease the address by one and examine the content Increase the address by one and examine the content
Start	Run the program
Single step	Run the program with one instruction per command

Each of these operations is caused by setting a certain combination of the lower four function switches and then pushing the corresponding push-button. "Load the address", "deposit a constant", and "examine the content" will cause interruption of the computer and these operations are done by corresponding interrupt service routines.

Peripherals*

Peripherals included Teletype, eight bit A/D convertor, nine bit D/A convertor, clock and eight channel digital input. All these devices communicate with the computer body through the tristate Peripheral Data Bus, which is terminated at port B of 8255. A schematic is given in Figure 34.

*Equipment also borrowed from Digital Systems Laboratory.

Each device is operated by the computer body through a sequence of control signals. These signals are generated by dedicated peripheral service routines when they are called and decoded from port C of 8255 and the Auxiliary I/O.

1. Teletype and Teletype Interface

Teletype was used at the system developing and program debugging stages. After those stages programs are stored in the PROM and variable coefficients are stored in the RAM, and the whole system is operable without the teletype. Teletype could be connected or disconnected to the system very easily.

2. Eight Bit A/D Convertor with
Four-to-one Analog Multiplexer

It includes an eight bit D/A convertor and a successive approximate register (Am 2503). An analog four-to-one multiplexer is used at the input end and controlled by the service routine. Four different analog channels could be sampled. A buffer is used at the output end to make the output tristate. The input range is from -2.5V to +2.5V, with corresponding output range from 00 to FF.

3. Nine Bit D/A Convertor with
Two Sample-and-hold Circuits

A buffer is used at the input end to reduce the load of the D/A convertor to the Peripheral Data Bus. Nine bit D-type flip-flops (five of 7474) are used as latches following the buffer. Two sample-and-hold circuits are implemented at the output end of the D/A convertor and are separately controlled by the service routine. The output range is from 0V to 5V, with corresponding input values 0000 to 01FF.

4. Clock and Digital Input

The clock is a synchronous eight-bit counter (two of 74161). The input pulses are generated by the 8224 clock generator, with frequency reduced by an adjustable factor to fit different applications. The output of the counter goes into one set of a data selector (set A) to make the output tristate. The other set of input of the data selector (set B) is used as digital input device for the system (eight channels), which is used to test different operation conditions. Peripheral service routines will be discussed in the next section.

Software Development

The software development began as soon as the computer body had been built. It could be divided into several stages: 1) Console monitor; 2) Peripheral service routines; 3) Loader and dumper; 4) Arithmetic routines; and 5) Control programs.

1. Console Monitor

Front panel operations are performed by this program. This is the most basic program which puts the computer body into operation. Basically it includes the RESET routine and two interrupt service routines. Interrupts are caused by pushing either the ADDRESS or the DATA push-buttons of the front panel. Flow charts are given in Figures 35, 36 and 37.

2. Peripheral Service Routines

These routines carry out the proper operation of all the peripherals, including teletype, A/D convertor, D/A convertor, clock and digital input. They monitor the operation of peripherals through the first three channels of the digital input and give appropriate commands through Peripheral Control Bus. They are strongly dependent upon the hardware structure of the computer. These routines are called each time some program wants to perform certain peripheral operations. The main program does not need to worry about the detail operations of the peripherals again.

a. TTYIN: The computer receives a character from the teletype and puts it into the accumulator.

b. TTYOUT: The computer sends the character in the accumulator to the teletype.

c. A/D: Select an analog channel, convert the signal-to-digital form and store in the accumulator.

d. D/A: The 9 bit data, which is stored in the lower part of the register pair HL, is sent to the D/A convertor. The selected sample-and-hold circuit then samples and holds the resultant signal.

e. Time: Read the clock into the accumulator.

f. RESCLK: Reset the clock.

g. TEST: Check the selected channel of the digital input device to see whether it is 1 or 0.

3. Loader and Dumper

These are design and debugging tools. The loader could load a program from punched paper tape into the RAM with a specified starting address. On the other hand the dumper dumps the content of the specified memories (include PROM and RAM) onto the teletype and paper tape. By using loader, dumper and front panel operations a program could be written and debugged very easily. The flow chart of the loader and the dumper are given in Figures 38 and 39.

4. Arithmetic Routines

Since it is essential to have an accuracy more than eight bit in the position control application and the 8080 is an 8 bit machine, double precision arithmetic is adopted in most cases. Floating point operations are desired, but they are too slow when done with software; therefore, fixed point arithmetic is used. Several subroutines were written in order to perform addition, subtraction, multiplication and other arithmetic operations.

a. Addition, subtraction, shift left and shift right (with or without sign extension)

   These operations are expanded into double precision arithmetic in a pretty straightforward way.

b. Unsigned multiplication: BC ← DE * L*

   Data stored in the register L and the register pair DE are treated as unsigned numbers; i.e., the eight bit content of L represents a number from 0 to 2^8-1 (255), and the sixteen bit content of DE represents a number from 0 to $2^{16}-1$. The contents of DE and L are multiplied together and the result is stored in the register pair BC. We know $2^{16} * 2^8 = 2^{24}$, the result should be of 24 bits. However, BC is only 16 bits and we do not want to go into a triple-precision mode either. As the result, it adds a limitation to this multiplication program: the result should be less than 16 bits; otherwise, overflow would occur. The flow chart is given in Figure 40.

---

*B,C,D,E,H,L are registers of 8080 and can be used as register pairs as BC, DE, HL.

5. Control Programs

The control programs are exactly the same for both lift and pitch degrees of freedom. Integrators are not included for the sake of simplicity. From Figure 21 the function of the computer is:

a. Reset the clock and sample the model position signal (y) from the A/D convertor.

b. Calculate the result of the second order difference equation:

$$z(n) \leftarrow b_o y(n) + z^*(n), \text{ where}$$

$$z^*(n) = a_1 z(n-1) + a_2 z(n-2) + b_1 y(n-1) + b_2 y(n-2)$$

and $z^*(n)$ has been calculated in the previous cycle (step 7)

c. Sample the position command signal (y) and calculate the compensated error signal: $e \leftarrow r - z(n)$

d. Sent output (e) through the D/A convertor.

e. Update data: Present state becomes previous state .... and so forth; that is,

$$z(n-1) \leftarrow z(n)$$
$$z(n-2) \leftarrow z(n-1)$$
$$\vdots$$
$$y(n-2) \leftarrow y(n-1)$$

f. Calculate $z^*(u)$

$$z^*(n) \leftarrow a_1 z(n-1) + a_2 z(n-2) + b_1 y(n-1) + b_2 y(n-2)$$

g. Check time and go back to step 1.

The flow chart of the program is given in Figure 41. Several things are worth mentioning:

1) Scaling of numbers: all inputs (y and r from A/D convertor) are 8 bit long and the coefficients a_i and b_i are scaled to 8 bit long too. With scaling factor equal to 16, the binary number 00000001 is equivalent to 0.0625 of the real number. Scaled coefficients of the compensators for lift and pitch degree of freedom are given in Table 3.

2) Since the input range of the A/D convertor is from -2.5V to +2.5V, and output range of it is from 00 to FF, a DC constant (80) Hex is inherently added to all the signals by the convertor. Instead of taking this constant out immediately after conversion, we do something else. We know that the value we really want is:

$$z(n)=a_1z(n-1)+a_2z(n-2)+b_0y(n)+b_1y(n-1)+b_2y(n-2)$$

However,

$$a_1(z(n-1)+80)+a_2(z(n-2)+80)+b_o(y(n)+80)+b_1(y(n-1)+80)$$

$$+b_2(y(n-2)+80)-(a_1+a_2+b_0+b_1+b_2-1)*80=z(n)+80$$

Instead of subtracting the quantity 80 right after A/D conversion, we could have every variable biased with this DC number. In this fashion all inputs are forced to be positive numbers, which will simplify the use of unsigned multiplications. The constant 80 will be cancelled out when z(n)+80 is subtracted from the position command, which is r+80, to get the position error signal e.

The time required for each complete calculation; i.e., the time from the first clock-reset to the next clock-reset, is about 4.4 milliseconds. Since the sampling frequency is 33.3 Hz for the lift degree of freedom and 100 Hz for the pitch degree of freedom, the two control programs could be run simultaneously, with the arrangement shown in Figure 42.

Hybrid Simulation in Real Time
Using the Microcomputer

After completion of the minicomputer the hybrid simulations which had been previously conducted at reduced speed were repeated in real time using the microcomputer instead of the PDP 11/10. In order to obtain the necessary speed, calculations were performed in fixed point arithmetic

Table 3

APPROXIMATION FOR THE COEFFICIENTS OF THE DIFFERENCE EQUATION

$$z(11)=a_1 z(n-1)+a_2 z(n-2)+b_o y(n)+b_1 y(n-1)+b_2 y(n-2)$$

	Coefficient	Designed Value	Scaled Value in Decimal	Scaled Value in Hex	Decimal Number which the Scaled Number Represents
Pitch	a_1	.84019	13	0D	.81250
	a_2	.09856	2	02	.125
	b_0	1.09073	17	11	1.0625
	b_1	1.05239	17	11	1.0625
	b_2	.22003	4	04	.25
Lift	a_1	.22024	4	04	.25
	a_2	.15984	3	03	.1875
	b_0	8.0853	129	81	8.0625
	b_1	8.8138	141	8D	8.8125
	b_2	2.1086	34	22	2.125

and the integrator in the forward path was eliminated.* This produced essentially the same step responses in real time that had previously been obtained at reduced frequency. In these real time tests the sampling frequencies were 33.3 Hz in lift and 100 Hz in pitch.

Step response of the lift degree of freedom for K=150 is given in Figure 43. The position signal is pretty noisy, which might be caused by the following reasons:

1. Quantization errors of coefficients
2. Truncation errors caused by fixed point arithmetic
3. Noise from A/D convertor

*The programs are listed in Appendix B for both the lift and pitch degrees of freedom.

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Chapter VI

A DIGITAL CONTROL DEMONSTRATION USING THE ONE-DIMENSIONAL BALANCE SYSTEM

Because the MIT-NASA prototype system is very complex and is also in frequent use for aerodynamic tests, it was decided to conduct initial tests of the digital control system using the one-dimensional demonstration balance. This magnetic balance is completely independent of the other magnetic balance systems and was used to demonstrate the ability of the microcomputer to perform actual digital control of a magnetic balance. The control software was rewritten to conform to the Aerophysics Laboratory one-dimensional magnetic balance system which has been used as a demonstration unit.

The schematics of the coil and the system are shown in Figure 44. In this case the magnetic field was generated by a single coil, with the axis vertical. The model, which was a ferromagnetic ball, was hung underneath the coil, the lateral position of the ball being maintained on the coil axis by the natural stability in this plane. The vertical displacement on the other hand was unstable open-loop. Closed-loop control was thus required. The microcomputer was used here as a digital compensator for the vertical direction. On-line implementation was made and the digital system performed well in all respects and indeed better than had the previous analog system.

1. System Description

The transfer function of the coil was a first order lag with the pole at -38.98 rad/sec. The transfer function of the model relating the position of the ball to the current in the coil was derived as follows:

F: force, position upward

X: position, position upward measured from center of coil

X_0: nominal equilibrium position

ΔX: $X-X_0$

I: current through the coil

I_0: nominal operating current

ΔI: $I-I_0$

K: a proportionality constant

M: mass of the ball

From the experiment we know: $F = \frac{KI^2}{X^2}$ 6.1

$$\Delta F = \frac{2KI\Delta I}{X^2} - \frac{2KI^2\Delta X}{X^3} = M\Delta\ddot{X} \qquad 6.2$$

$$\Delta\ddot{X} + \frac{2KI_0^2}{MX_0^3}\Delta X = \frac{2KI_0}{MX_0^2}\Delta I \qquad 6.3$$

In the prototype case the ball is suspended below the coil with the nominal current required to overcome the gravity force. $I_0 = 90$ amp, $X_0 = -.084$m, and the transfer function is

$$\frac{\Delta\dot{X}}{\Delta I} = \frac{8.0 * 10^{-4}}{(1-\frac{s}{15.26})\ (1+\frac{s}{15.26})} \quad \text{(m/amp)} \qquad 6.4$$

The sign of the "spring" coefficient is negative, leading to the unstable mode.

We also notice that in the MIT-NASA magnetic suspension and balance system the corresponding transfer function for the lift degree of freedom is a double integrator, $1/s^2$. The reason for the difference is as follows: in the MIT-NASA system separate coils are provided to generate a uniform model magnetizing field and a separate gradient field. The magnetic supporting force is proportional only to the gradient field; i.e., F is proportional to the current through the gradient coil only. In the demonstration case there was only one coil which generated both the magnetizing and the gradient fields, and force was proportional to the square of the current and inversely to the square of the distance.

In addition to the coil, the ball and the microcomputer several other components were included in the system:

Position sensor -- It consisted of a light source and a photocell. The operation of this position sensor is best explained by Figure 45. The output of the photocell was proportional to the illuminated area, and varied from zero to two hundred millivolts. To obtain a ± directional reference, a bias signal was provided.

Power amplifier -- This was a Torque System Incorporated Model PA-601 operational power amplifier. The transfer function of the power amplifier was a pure gain, which was set to a value of two.

Generator -- This was a General Electric 2CM73B7 generator, running at 3500 RPM. With field voltage as the input and armature voltage as the output, the transfer function was

$$G(s) = \frac{2.86}{1 + \frac{s}{8.39}} \quad \text{volts per volt} \qquad 6.5$$

Interface box -- The input range of the eight bit A/D convertor was from -2.5 volts to +2.5 volts; the output range of the nine bit D/A convertor was from 0 volt to 5 volts; and the output of the photocell was from 0 volt to 0.2 volts. Interface circuits were needed in order to match the different ranges of different components. A DC bias voltage was also necessary to generate the DC bias current to hold the model at the operating point. The interface will be described in more detail in Section 4. It should be noticed that these interface circuits include only simple algebraic operations upon signals, such as addition of a constant, subtraction of a constant, or multiplication by a constant. There was no phase lead or lag. As the result, in the design of digital compensators we did not need to consider these circuits at all. The block diagram of the system is shown in Figure 46.

2. Synthesis of Compensators

After the transfer function of each component had been identified, the synthesis of a digital compensator follows the method described in Chapter III. The compensator is put in the feedback path. Two third-order compensators were designed as listed below:

a) zeros at 0.76427, 0.86728, 0.87893

poles at 0.13534, 0.25, 0.3, sampling frequency = 100 Hz and without integrator

b) zeros at 0.68008, 0.68008, 0.79161

poles at -0.13671, -0.18821, -0.25209, sampling frequency = 50 Hz with or without integrator

The Z-plane root locus for the first compensator is given in Figure 47.

Hybrid simulations using the microcomputer and the analog computer were carried out in the same manner as those described in Chapter IV prior to converting the microcomputer to the one-dimensional balance.

3. Structure of the Program

A third-order compensator was rewritten as three first-order compensators, as follows:

$$\frac{Z(z)}{y(z)} = \frac{K(z-b_3)(z-b_2)(z-b_1)}{(z-a_3)(z-a_2)(z-a_1)}$$

$$\equiv \frac{Z_3(z)}{y(z)} \equiv \frac{Z_3(z)}{Z_2(z)} \frac{Z_2(z)}{Z_1(z)} \frac{Z_1(z)}{y(z)} \qquad 6.6$$

$$= \frac{K_3(z-b_3)}{(z-a_3)} \frac{K_2(z-b_2)}{(z-a_2)} \frac{K_1(z-b_1)}{(z-a_1)}$$

and

$$Z_1(n)=A_1Z_1(n-1)+B_oy(n)+B_1y(n-1) \qquad 6.7$$

$$Z_2(n)=A_2Z_2(n-1)+B_2Z_1(n)+B_3Z_1(n-1) \qquad 6.8$$

$$Z_3(n)=A_3Z_3(n-1)+B_4Z_2(n)+B_5Z_2(n-1) \qquad 6.9$$

In the control program the compensator was calculated as three first-order compensators as above, with all the coefficients stored in the Random Access Memory.

If the integrator was added in the feed-forward path to reduce the long term drifting, as shown in Figure 46, it could also be treated as a first order difference equation as follows:

$$\frac{f}{e} = \left(1 + \frac{K_i T}{2}\left(\frac{1+z^{-1}}{1-z^{-1}}\right)\right) \qquad 6.10$$

$$= \frac{\left(1 + \frac{K_i T}{2}\right) - \left(1 - \frac{K_i T}{2}\right) z^{-1}}{1 - z^{-1}}$$

$$Z_4(n) \triangleq f(n) = A_4 Z_4(n-1) + B_6 e(n) + B_7 e(n-1) \qquad 6.11$$

where:

$$A_4 = 1,\ B_6 = 1 + \frac{K_i T}{2},\ B_7 = \frac{K_i T}{2} - 1 \qquad 6.12$$

The flow chart of the program is given in Figure 48. Whether the integrator was used or not was set by the second DATA SWITCH on the front panel. It was monitored by the program continuously.

The control program is listed in Appendix C.

4. Interface Circuits Control

As described in Section VI-1, three interface circuits were used in order to match different operating ranges and to add the bias current to the coil. The open loop gain was also adjusted in one of the circuits. Schematic of the system including interface circuits is given in Figure 49.

a) Interface A (IFA): this received signal y' from the position sensor and gave the resultant signal y to the A/D convertor.

Input range (y'): 0 to .2 volts

Desired output range (y): -2.5 volts to +2.5 volts

Transfer function: $y' = -25\ (y - 0.1)$

b) Interface B (IFB): this received the compensated error signal from the D/A convertor (f) and sent the resultant signal (f') to the power amplifier. It also included the open loop gain adjustment and added a DC bias voltage to the signal to generate a bias current.

Input range (f): 0 to 5 volts

Desired DC bias: 3.6 volts

Transfer function: $f' = -(K(f-2.5)+\text{DC bias})$

c) Interface C: it is an input summing stage. It could sum two input signals and also include an ON-OFF toggle switch.

It was possible to operate the entire system successfully. Suspension was stable and measurements were made of response to step input and the response to sinusoidal perturbation signals. Model position (y') compensated error signal (f) as well as coil current (i) were recorded. Several step responses with sampling frequency equalled to 100 Hz are given in Figure 50.

5. Points Suggested by the Experiment

As a consequence of the experimental program there is increased confidence in the feasibility of digital controls with their many advantages. At the same time several things become apparent which are not likely to have been discovered with only theoretical analysis. These are summarized as follows:

a) A fast processor is essential at the beginning if non-linear and adaptive controls are to be considered, since a high sampling frequency will be needed. Thus the computation time available is short and more computation than used in this investigation will be needed.

b) A floating point processor is desirable if the control range is to be increased and if non-linear and/or adaptive controls are needed. This is necessary to avoid scaling limitations.

c) In the design of digital compensators phase lead should be minimized to reduce the amplification of noise introduced in the measurement and sampling operations.

d) Means of recording, controlling and documenting software are essential.

Chapter VII

ATTAINABLE LIMITS OF ACCURACY OF MODEL LOCATION AND ATTITUDE

The attainable limits of accuracy of model location and attitude depend upon the limits of analog-to-digital convertors, digital-to-analog convertors, the way of arithmetic calculations and the word length of the processor used. In this chapter a rough estimation is made by assuming a typical minicomputer with 16 bit word length is used.

From the calibration data of Equation 2.1, sensitivities of the EPS are:

lift	337.2 mv/inch
drag	540.0 mv/inch
pitch	16.4 mv/degree
yaw	27.8 mv/degree

2000 mv of EPS output, which allows movement of 5.93 inches in lift axis, 3.70 inches in drag axis, 122.0 degrees in pitch and 71.9 degrees in yaw is temporarily assumed to be good enough for the present analysis.

If an eight bit analog-to-digital convertor were used, with the full range from zero to 2000 mv, one bit would represent 7.8125 mv, or 2.3169×10^{-2} inches for lift degree of freedom. Table 4 is thus obtained by similar reasoning. With 12 bit analog-to-digital convertors, which are commercially available at reasonable prices, one could have fairly good resolution.

Either fixed point arithmetic or floating point operation could be used. With a steady state sensitivity of the digital filter equal to one, the digital processor is assumed to be able to calculate the compensated error signal without overflow. We also assume the truncation error caused by the finite word length is not serious.

Assuming a 12 bit analog-to-digital convertor is used, with 0.488 mv per bit, the maximum quantization error is 0.488 mv. To get a brief idea about the propagation of quantization error, please refer to Figure 51.

Table 4

RESOLUTION FOR DIFFERENT A/D CONVERTORS

Number of Bit of A/D	mv per Bit	Corresponding Movement			
		Lift (in)	Drag (in)	Pitch (deg)	Yaw (deg)
8	7.81	2.32×10^{-2}	1.45×10^{-2}	4.67×10^{-1}	2.81×10^{-1}
10	1.95	5.79×10^{-3}	3.61×10^{-3}	1.19×10^{-1}	7.03×10^{-2}
12	4.88×10^{-1}	1.45×10^{-3}	9.03×10^{-4}	2.78×10^{-2}	1.76×10^{-2}
16	3.05×10^{-2}	9.05×10^{-5}	5.65×10^{-5}	1.86×10^{-3}	1.10×10^{-3}

In Part a the quantization error is treated as an independent source, added to the system at the analog-to-digital convertor. The system could also be plotted, as shown in Part b. This system has identical eigen-values to the one in Part a and the only difference is the position of closed loop zeros. As a result the responses of the two systems are approximately the same. The maximum quantization is 0.488 mv; the position error caused by this error is of the same level and is a very small quantity when translated to inches or degrees.

It thus appears that the positional accuracy of a digitally-controlled MMSB will be limited by the analogue position signals generated by the EPS system if the computer is correctly designed.

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Chapter VIII

CONCLUSIONS AND RECOMMENDATIONS

The results of this feasibility study indicate that present day digital computers can successfully perform the magnetic balance control functions.

Actual operation of a digitally controlled one degree of freedom magnetic suspension system was demonstrated using a microcomputer constructed around the Intel 8080 processor. While sufficient for this feasibility study this processor is much too small for control of the full NASA prototype system. Even more capacity will also be required in order to perform data reduction and adaptive or non-linear control functions.

The initial experiments described have clearly demonstrated the utility of a digital microprocessor for performing the magnetic balance compensation functions in a linear control system. They have also indicated that use of a digital control system should lend itself to:

Automatic data reduction.

Accurately preprogrammed model motion.

Non-linear and self-adaptive control processes which might greatly improve performance

The next logical step is to incorporate a dedicated digital processor controller into the NASA prototype magnetic balance system and use it to develop the above areas. After software has been developed to handle the desired control loop and data reduction functions, a system could be specified that would be suitable for the 2.5m NTF or pilot .3m facility. One possible configuration is shown in Figure 52. The digital processor is divided into two subsystems, such that each of them could be installed using current computers at reasonable prices and the relationship between them is clearly defined.

A dedicated digital processor is used to do all the automatic control functions, including control of six channels of magnetic model suspension and balance system and the management of the wind tunnel. The other computer is used to collect and reduce experimental data and carry out research calculations involving aerodynamic experiments and the MMSB itself. The second computer should be operated at high level language for ease of communication with tunnel operators. It should also have adequate memory for future flexibility.

Another suggested structure is shown in Figure 53. One processor is used to do all the model control functions, including non-linear and adaptive control. The other processor is used to collect and reduce experimental data and manage the wind tunnel housekeeping.

Another option is that the data could be stored on disks and analyzed later, and only one processor is needed. A checklist for the selection of computers is given in Table 5.

Table 5

CHECKLIST FOR THE SELECTION OF COMPUTERS

I.	CPU	1. Architecture 2. Speed 3. Word Length 4. Instruction Set 5. Multi-Level Interrupt 6. Direct Memory Access 7. Floating Point Capability 8. Reliability and Maintainability 9. Memory Management 10. (Cache Memory)
II.	Peripherals	1. Terminal a. Teletype/DEC Writer b. CRT 2. Disk or Fixed Head Disk 3. Real Time Clock 4. A/D, D/A 5. (Line Printer) 6. (Floppy Disk)
III.	Software	1. Real Time Operating System 2. Language Processors 3. Diagnostic Software 4. (Multi-task, Multi-programming Operating System)
IV.	Future Expansion	1. Data Reduction 2. Tunnel Management 3. Multi-processor System
V.	Service	
VI.	Price	

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REFERENCES

1. Chrisinger, J E, "An Investigation of the Engineering Aspects of a Wind Tunnel Magnetic Suspension System", Massachusetts Institute of Technology, Aeronautical Engineering Thesis, TR 406, 1959.

2. Covert, E E, M Finston, M Vlajinac and T Stephens, "Magnetic Balance and Suspension System for Use with Wind Tunnels", Progress in Aero Space Sciences, Vol 14, Pergamon Press, 1973, pp 27-107.

3. Tournier, M and P Laurenceau, "Suspension Magnetique d'une Maquette en Soufflerie", La Recherche Aeronautique, No. 59, July-August, 1957, pp 21-27.

4. Tilton, E L and S Schwartz, "Static Tests of the Magnetic Suspension System", Massachusetts Institute of Technology, AR Memo 399, July, 1959.

5. Tilton, E L and L Baron, "Design, Construction and Testing of an Automatic Control System for a Wind Tunnel Magnetic Suspension System", Thesis for a B.S. Degree, Dept. of Aeronautics and Astronautics, Massachusetts Institute of Technology, May, 1960.

6. Stephens, T, "Design, Construction and Evaluation of a Magnetic Suspension and Balance System for Wind Tunnels", Aerophysics Laboratory Technical Report 136, Massachusetts Institute of Technology, November, 1969.

7. Tilton, E L, "Dynamic Stability Testing with a Wind Tunnel Magnetic Model Suspension System", Master's Thesis, Department of Aeronautics and Astronautics, Massachusetts Institute of Technology, January, 1963.

8. Whitaker, H P, "Development of a Parameter Optimization Technique for the Design of Automatic Control Systems", NASA Contract Report 143844, 1977.

9. Intel 8080 Microcomputer Systems User's Manual, September, 1975.

10. Luh, P B, "A Digital Control System for a Wind Tunnel Model Suspension and Balance System", S.M. Thesis, Department of Aeronautics and Astronautics, Massachusetts Institute of Technology, June, 1977.

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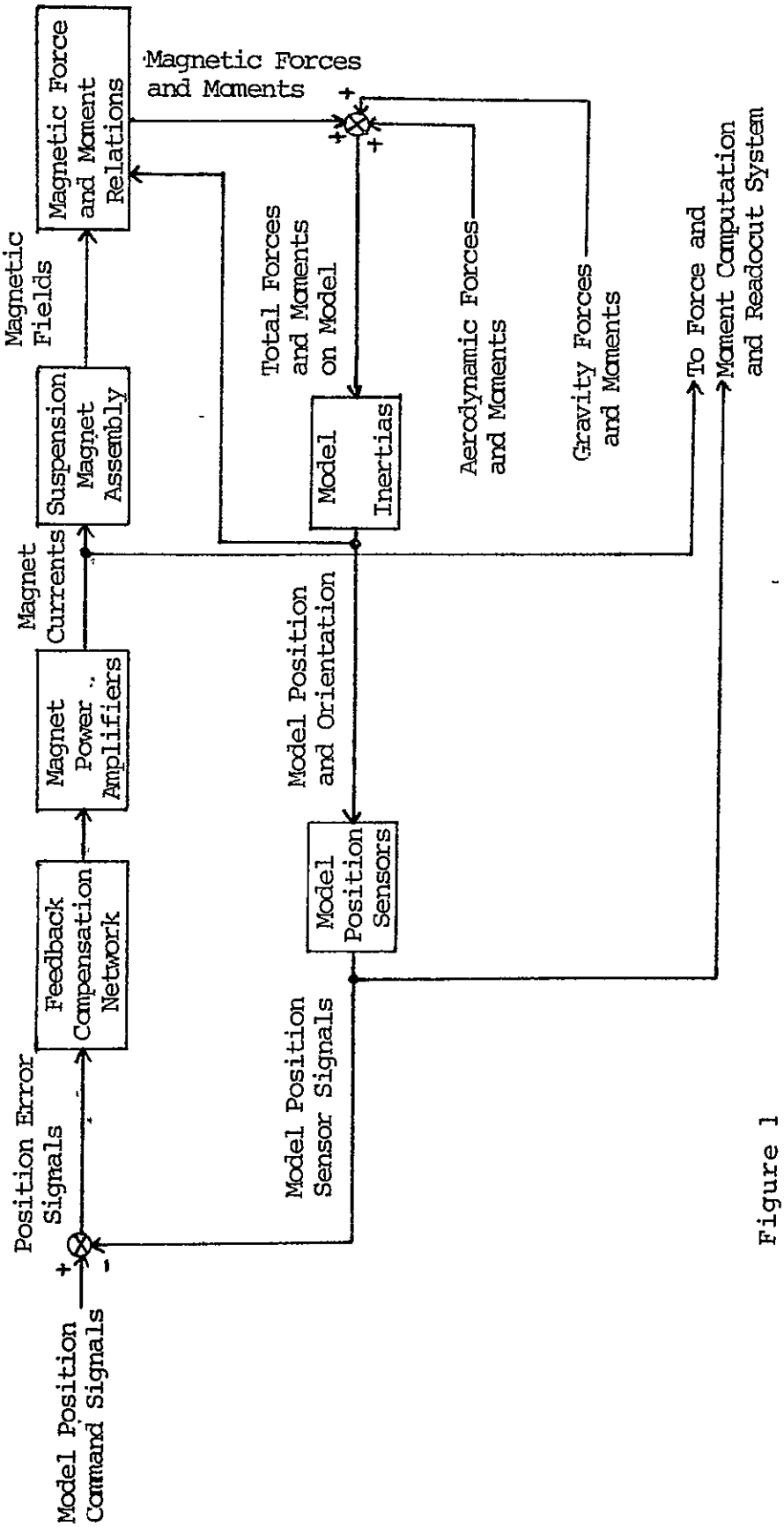


Figure 1

Functional block diagram of suspension system

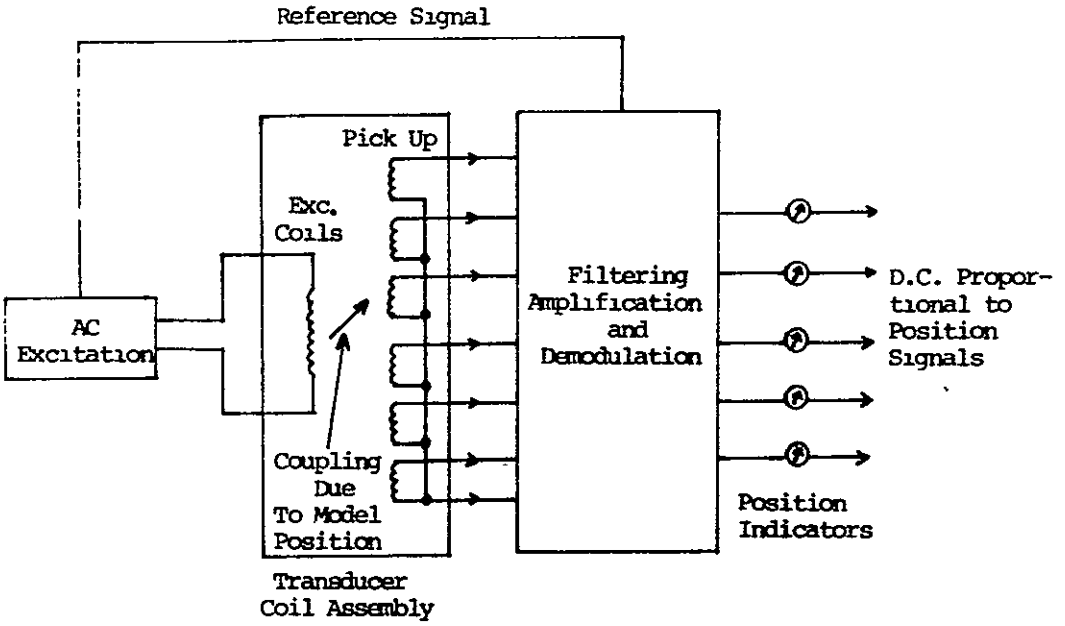


Figure 2 Electromagnetic Position Sensor (E.P.S.) system: simplified schematic

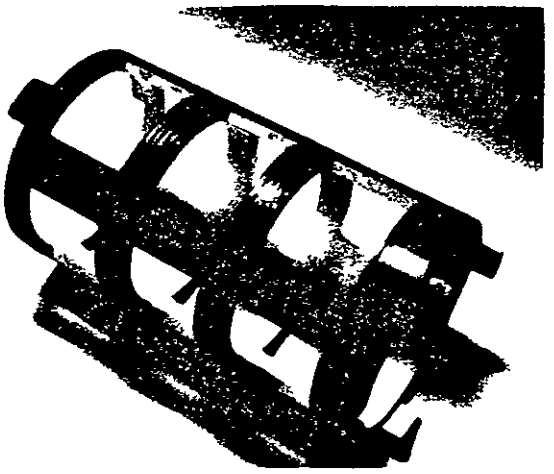
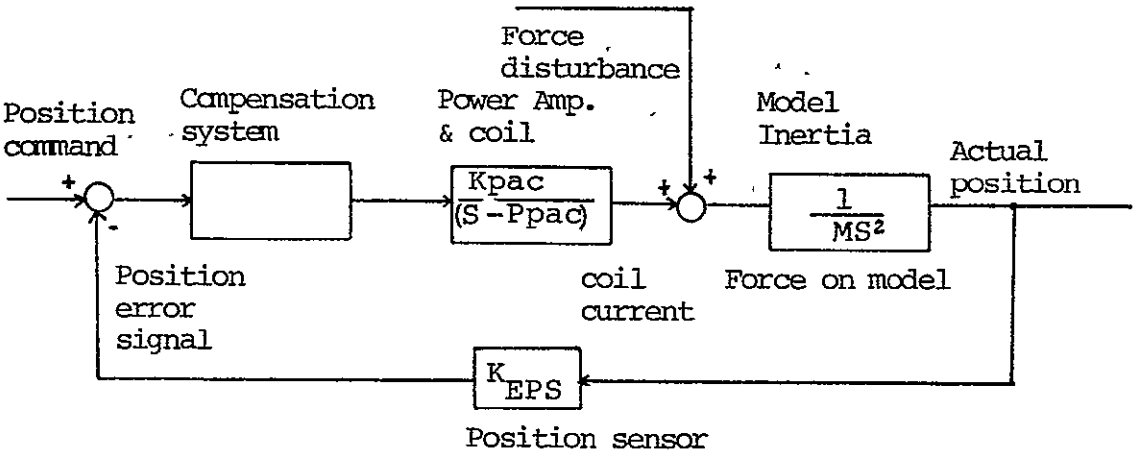
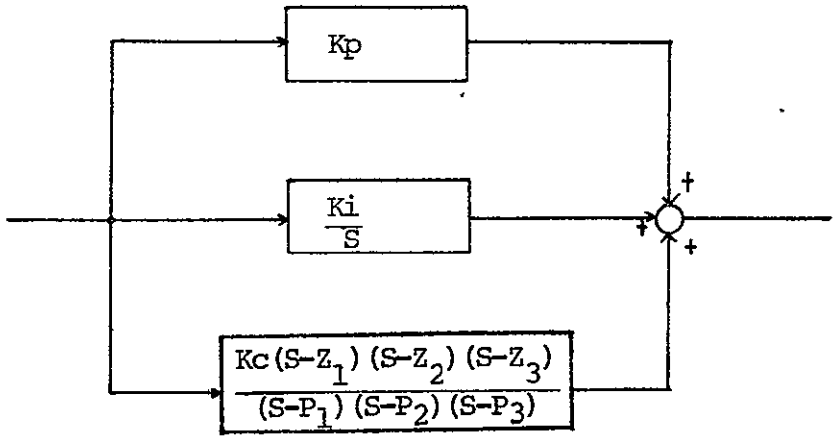


Figure 3 Prototype E.P.S. system transducer coil assembly



Figure

Servo-loop diagram of suspension system translational axis (lift, drag, slip)



Figure

Schematic of compensator

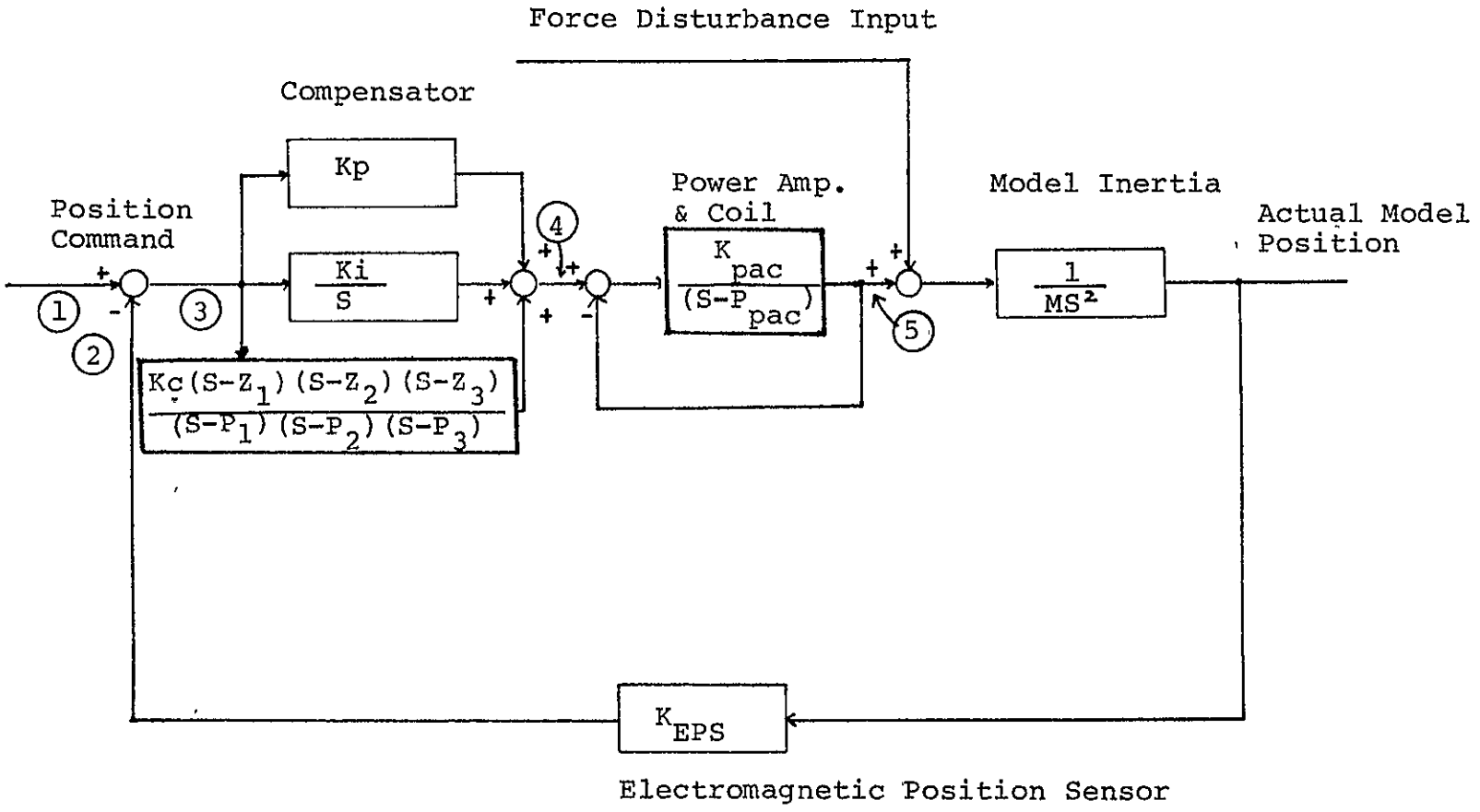


Figure 6

Servo loop diagram of suspension system, translational degree of freedom

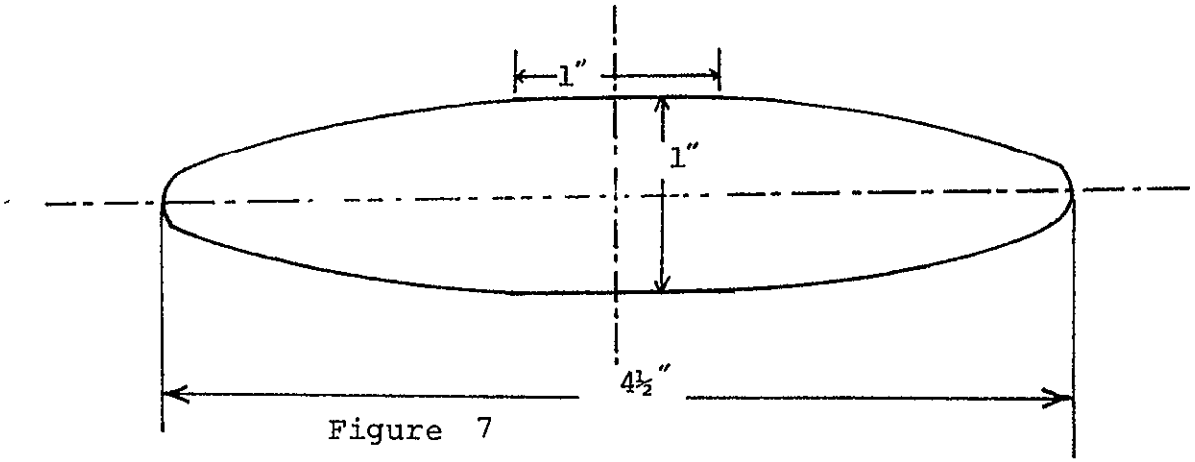


Figure 7
Copper-plated ellipsoidal core

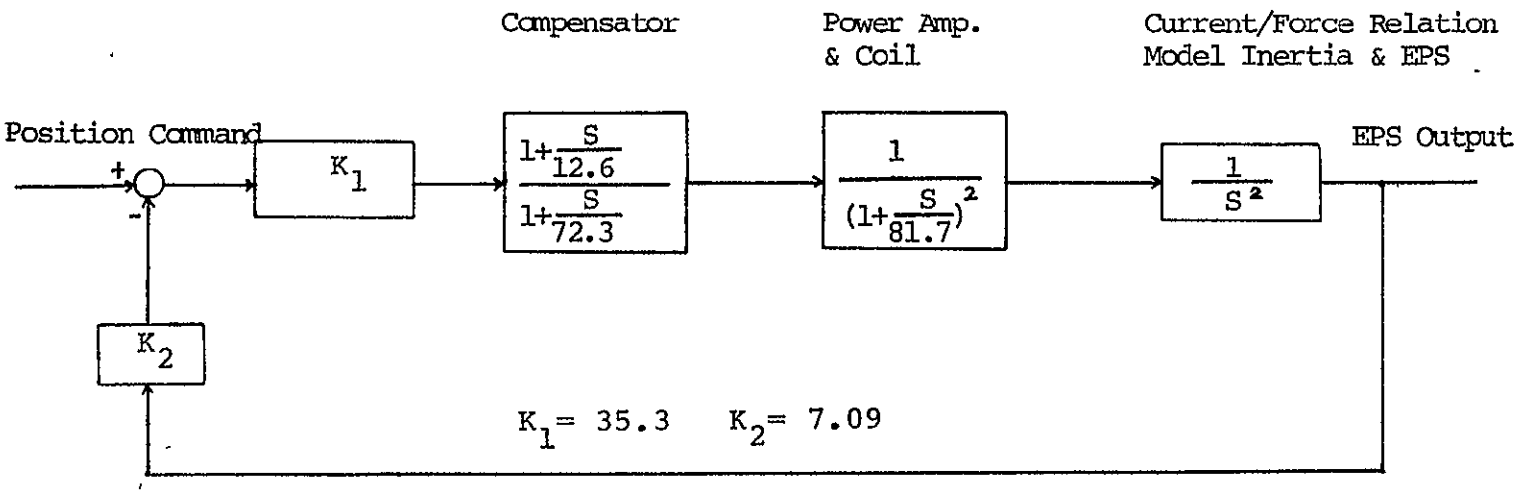


Figure 8 Block diagram of the lift degree of freedom

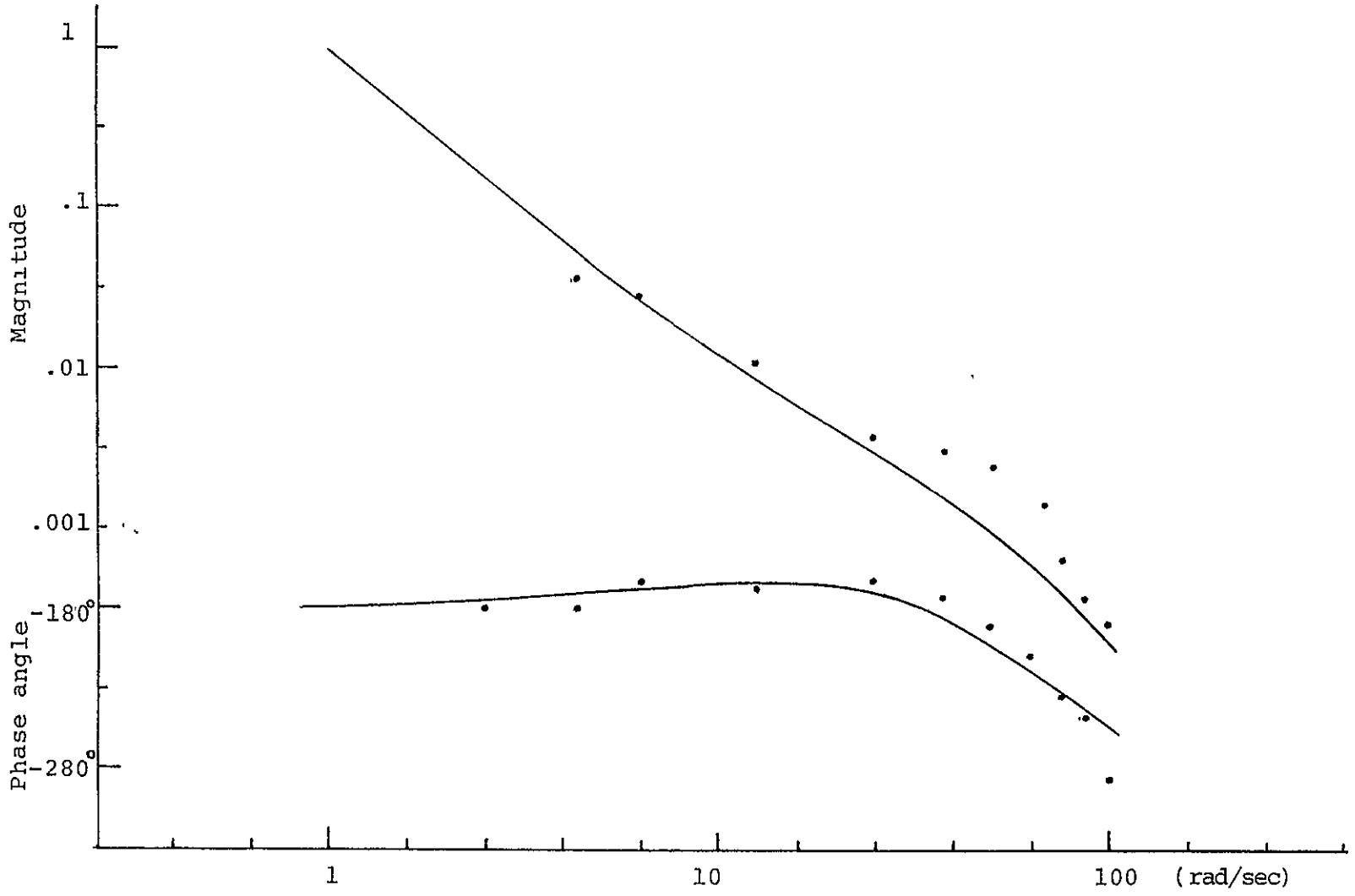


Figure 9

Lift degree of freedom open-loop Bode plot, 2/3.

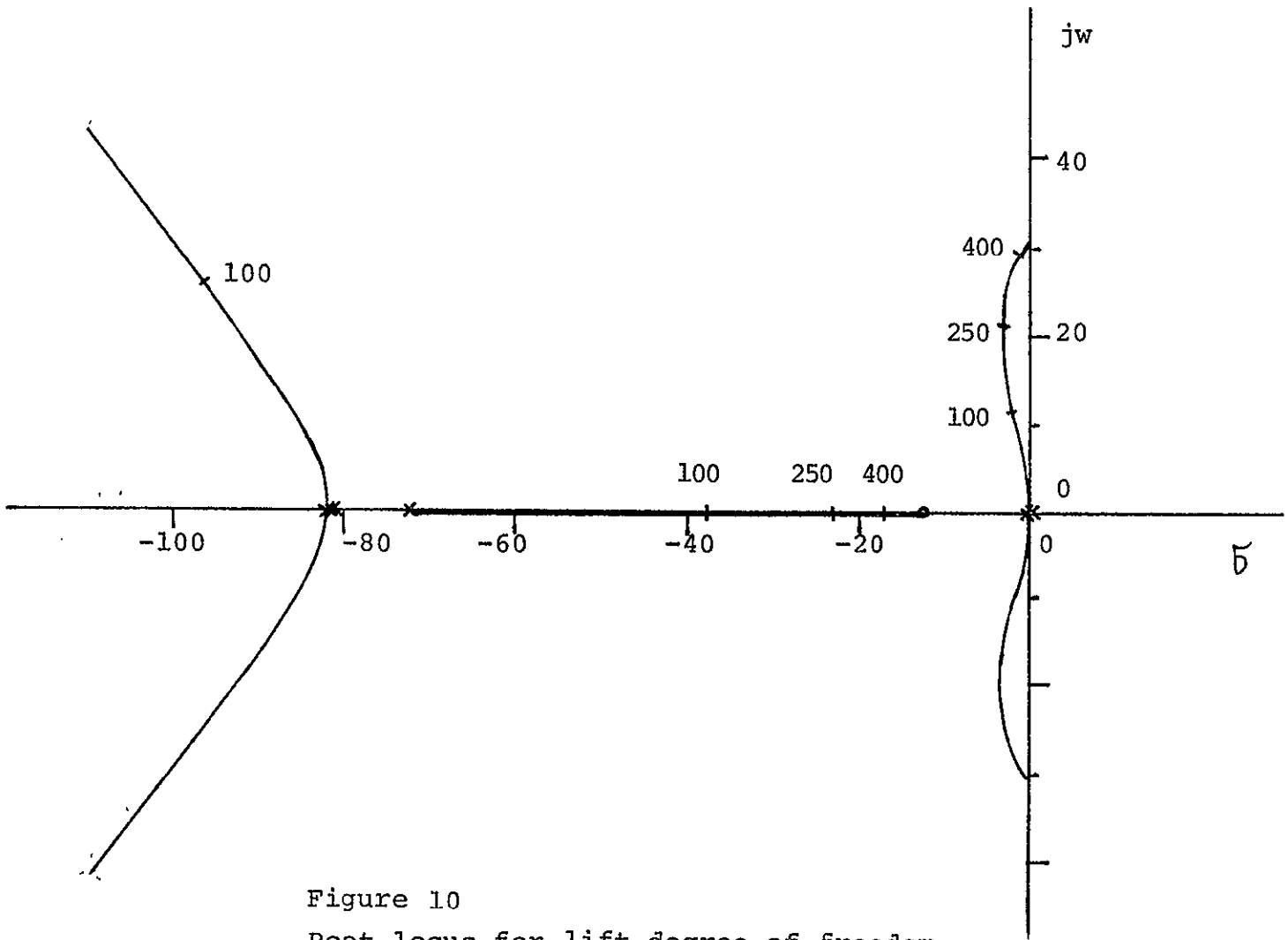


Figure 10
Root locus for lift degree of freedom

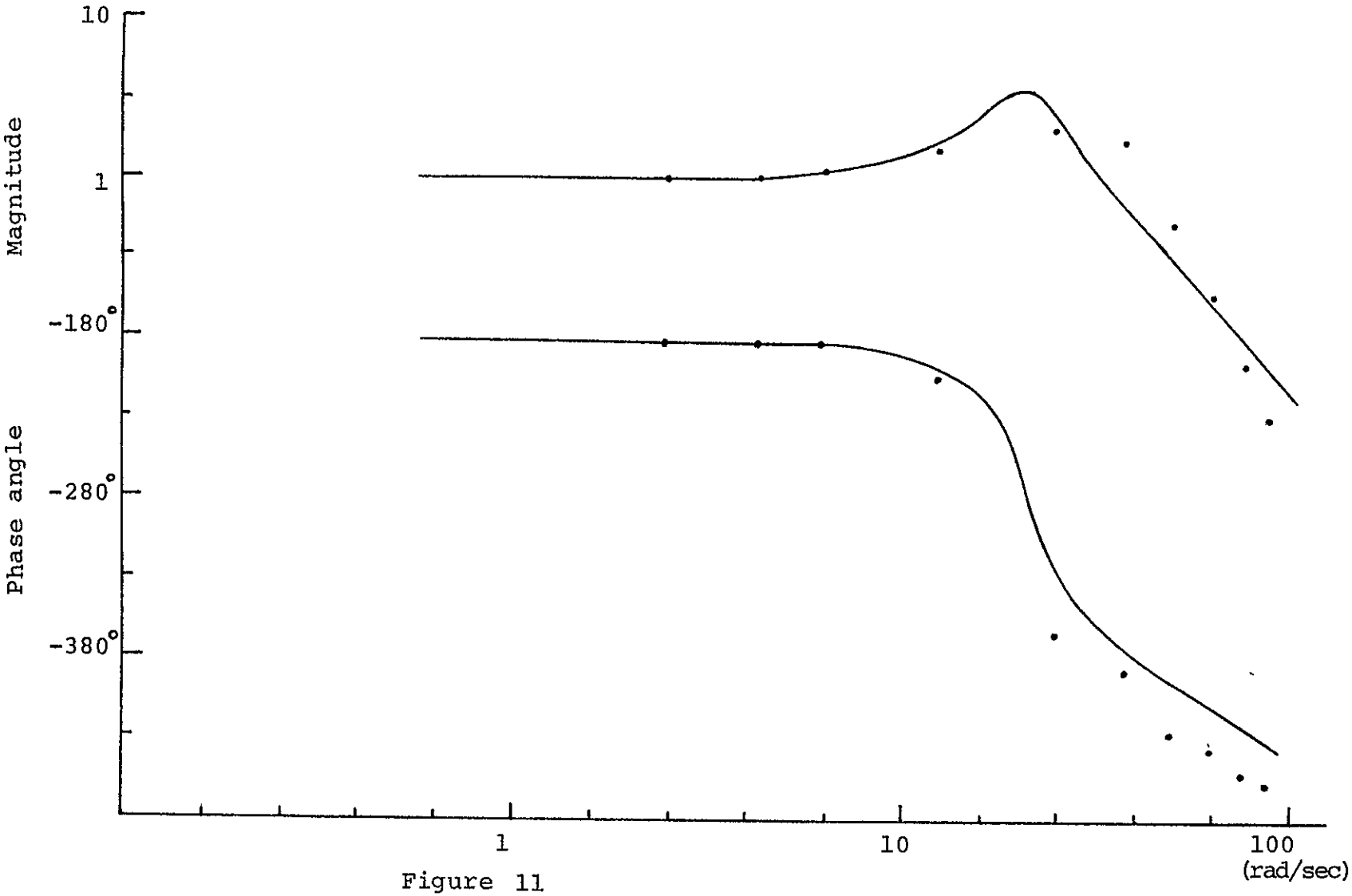
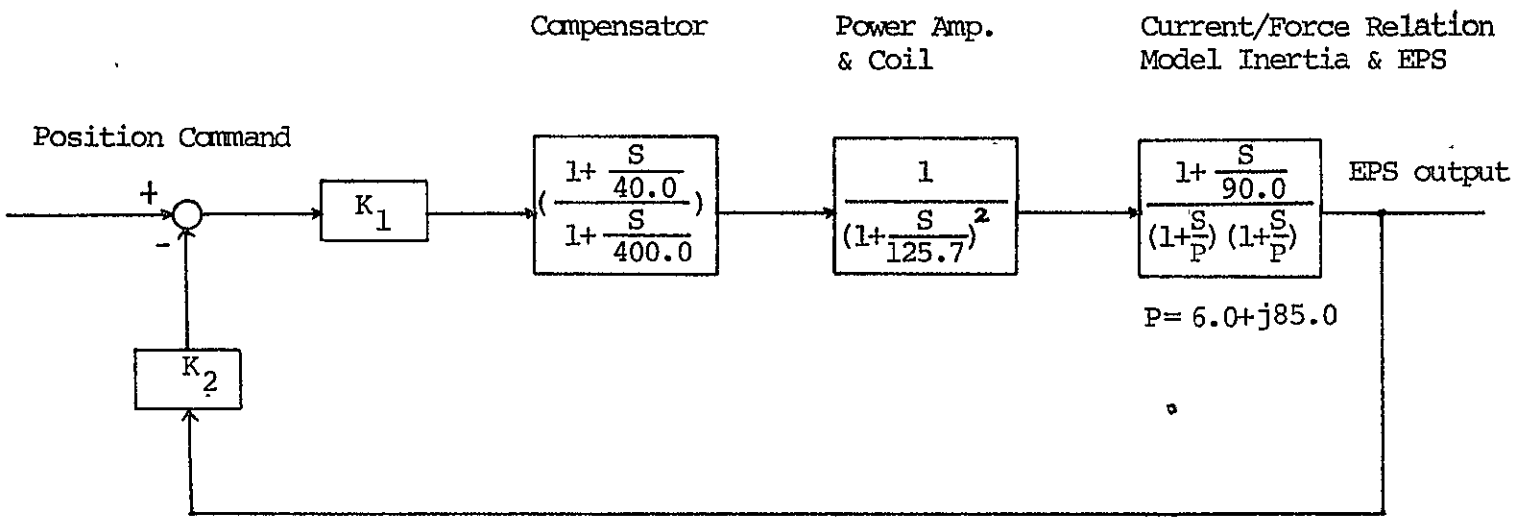


Figure 11

Lift degree of freedom closed-loop Bode plot



$K_1 = 0.083$

$K_2 = 0.53$

Figure 12

Block diagram of the Pitch axis

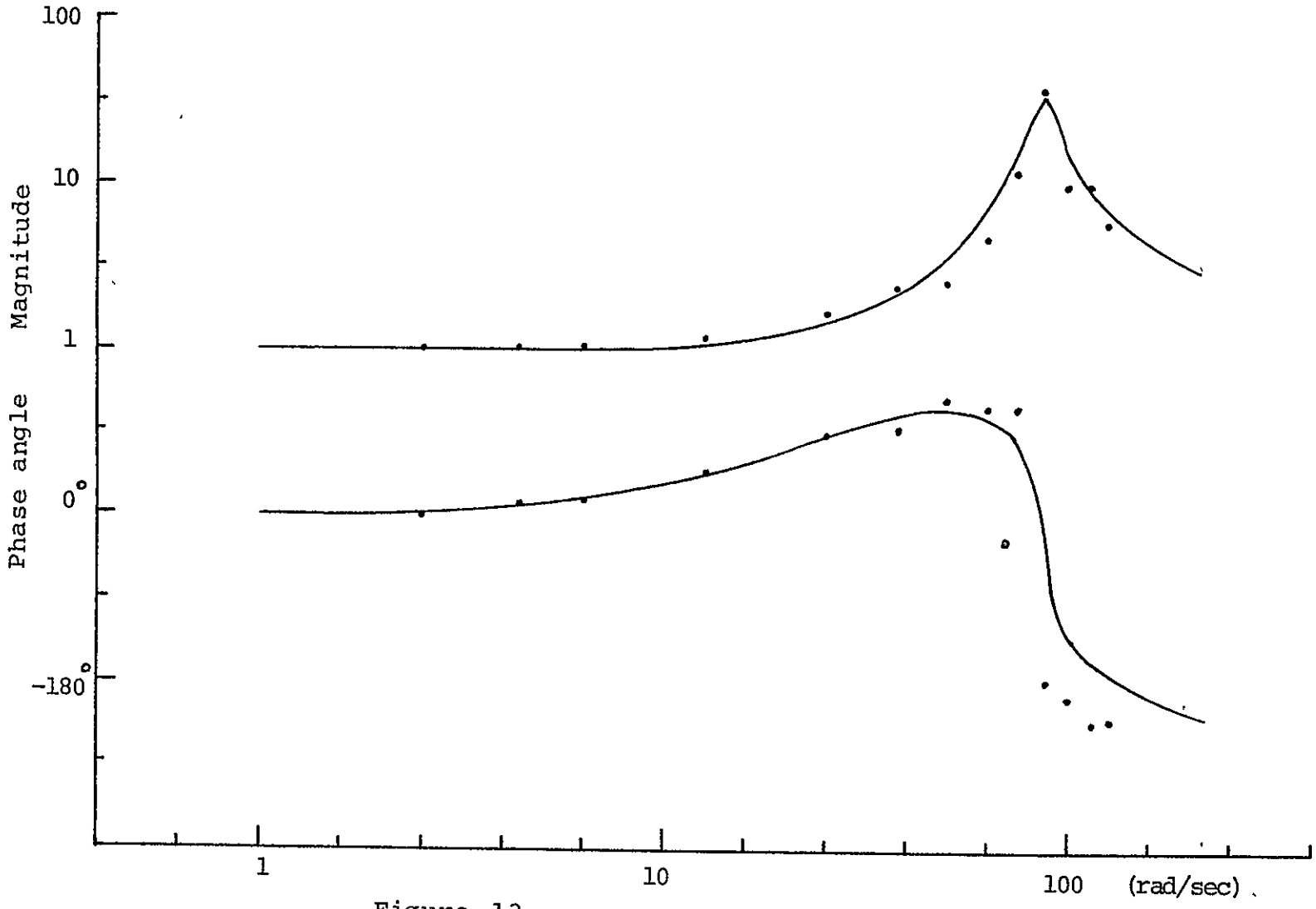


Figure 13

Pitch axis open-loop Bode plot, 2/3

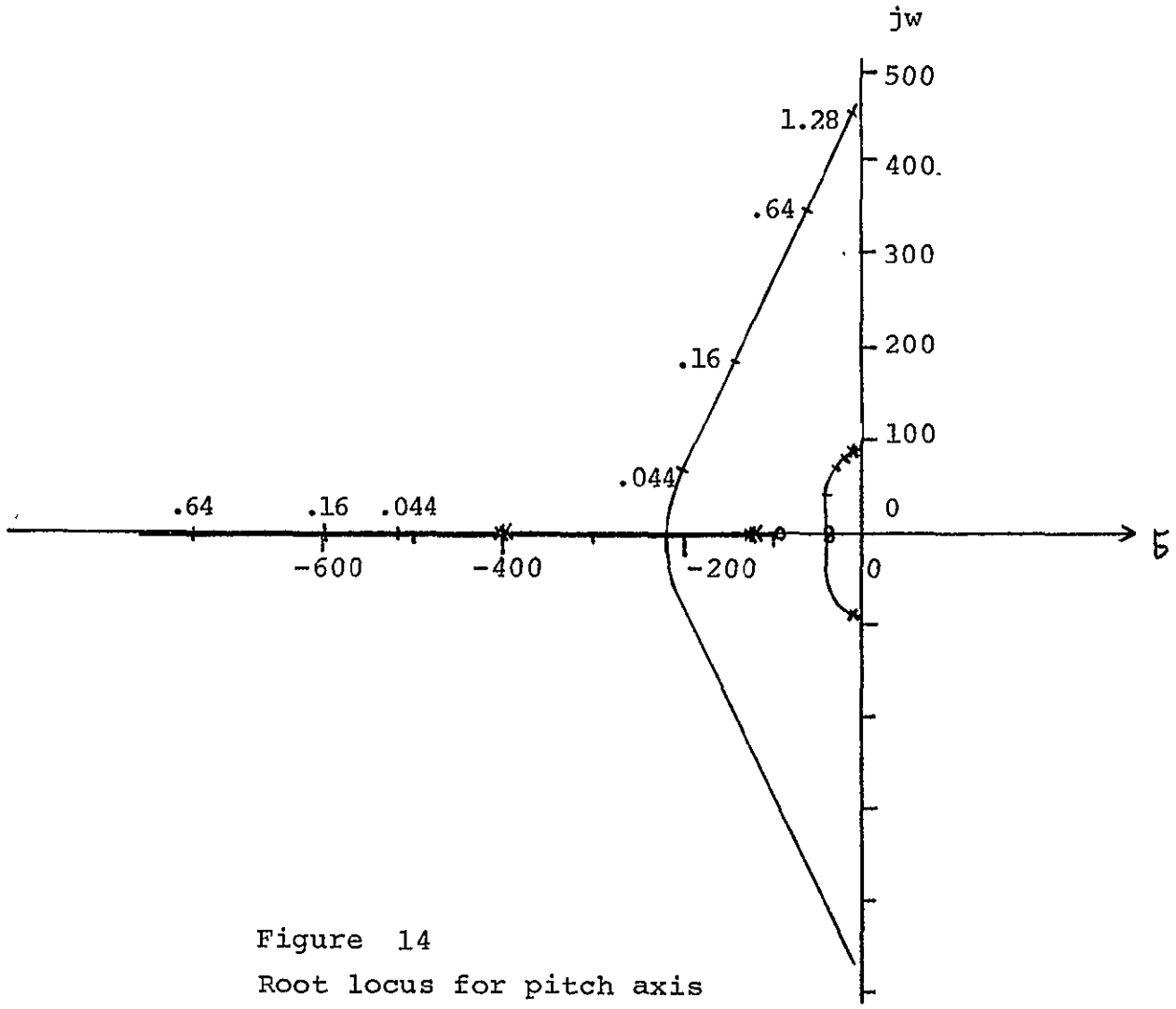


Figure 14
Root locus for pitch axis

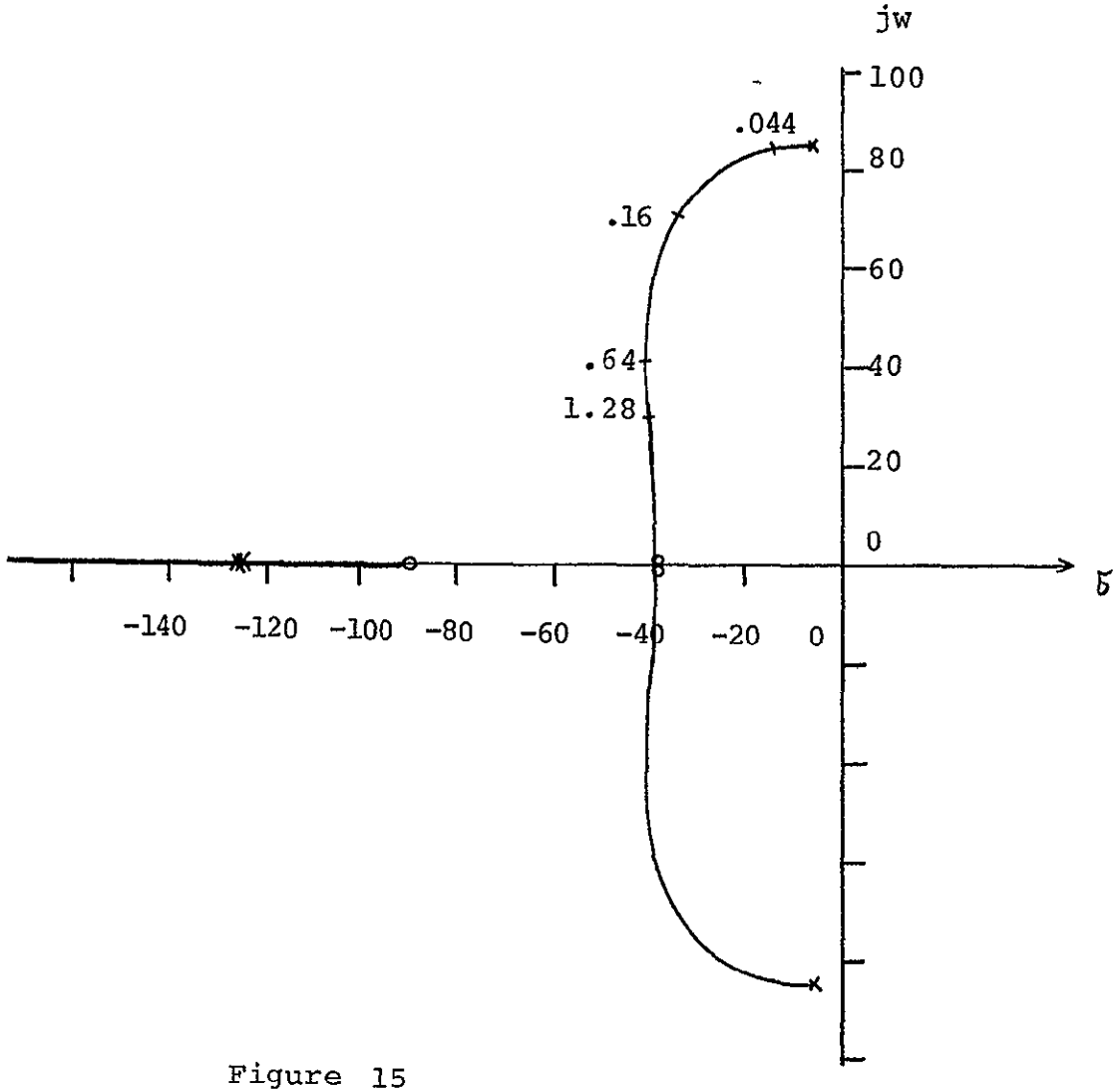


Figure 15
Root locus for pitch axis

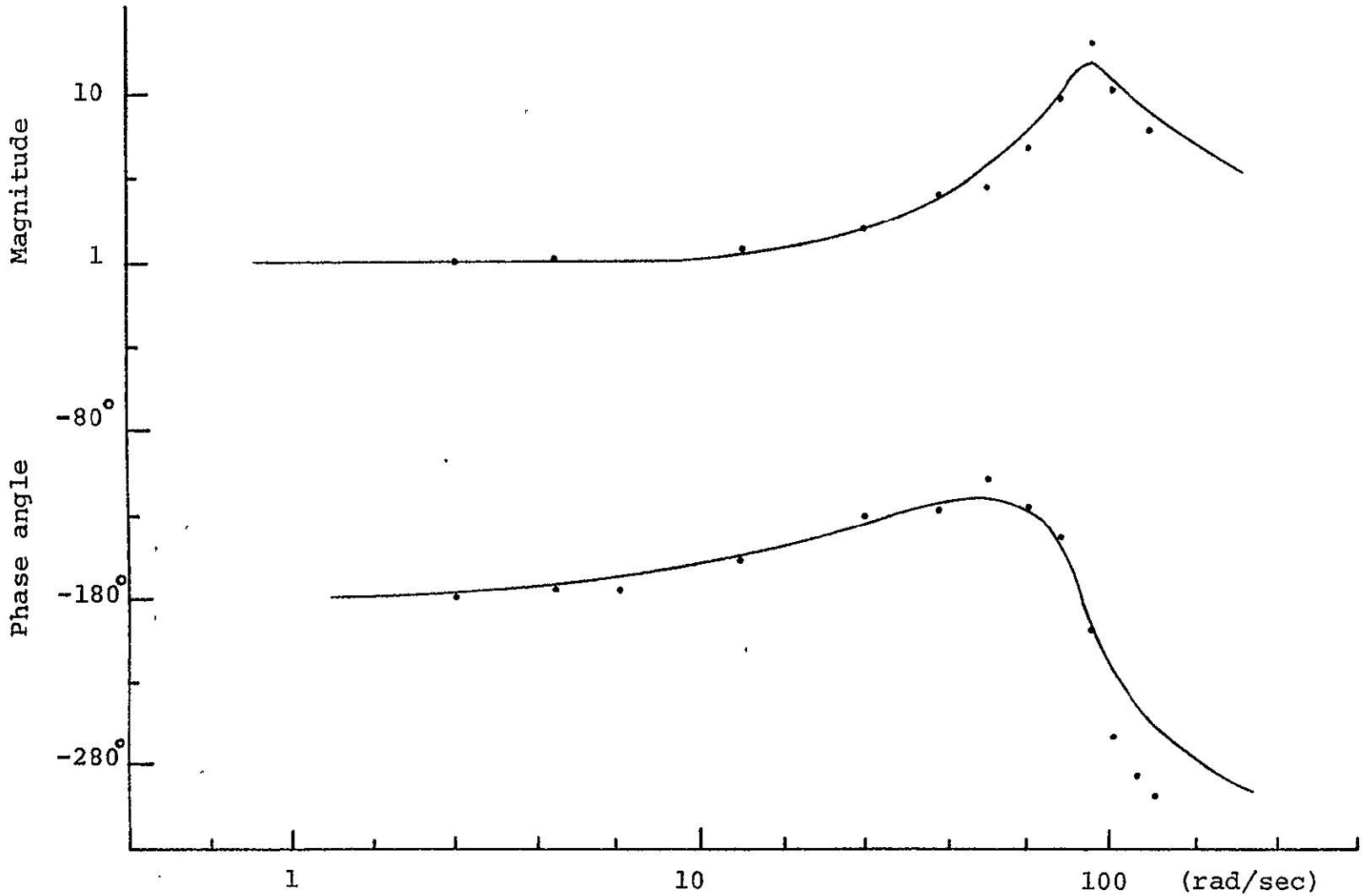
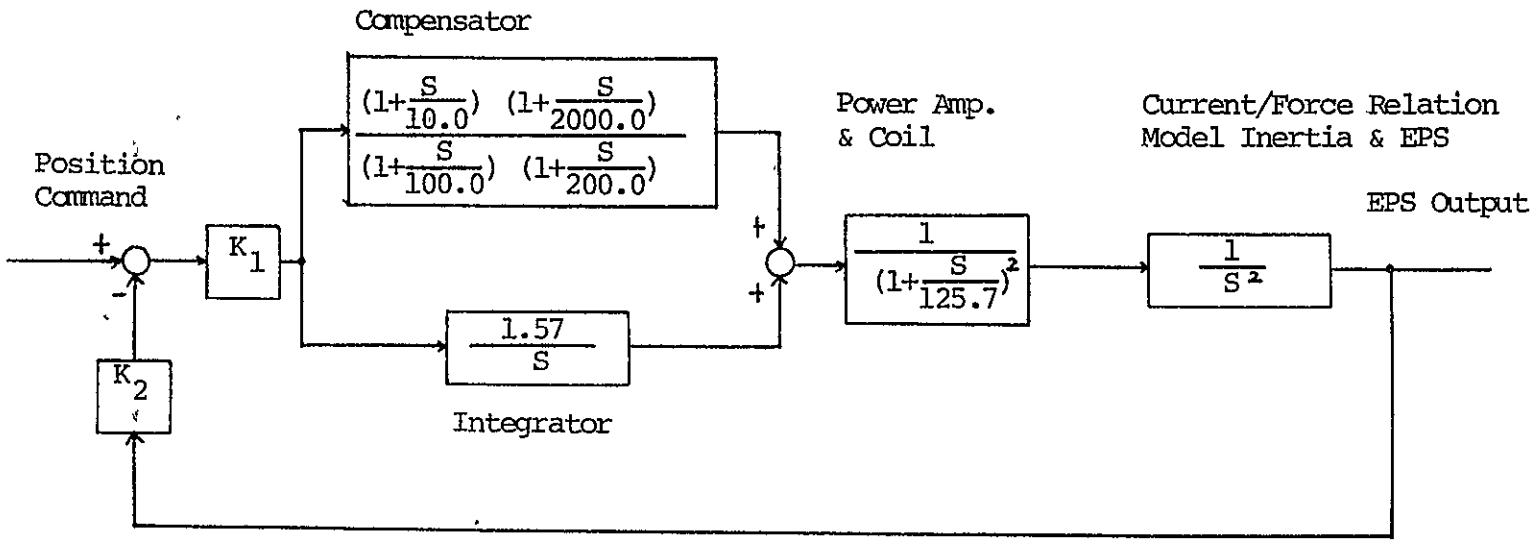


Figure 16

Pitch axis closed-loop Bode plot, 2/1



$K_1 = 53.4$

$K_2 = 5$

Figure 17

Block diagram of the drag degree of freedom

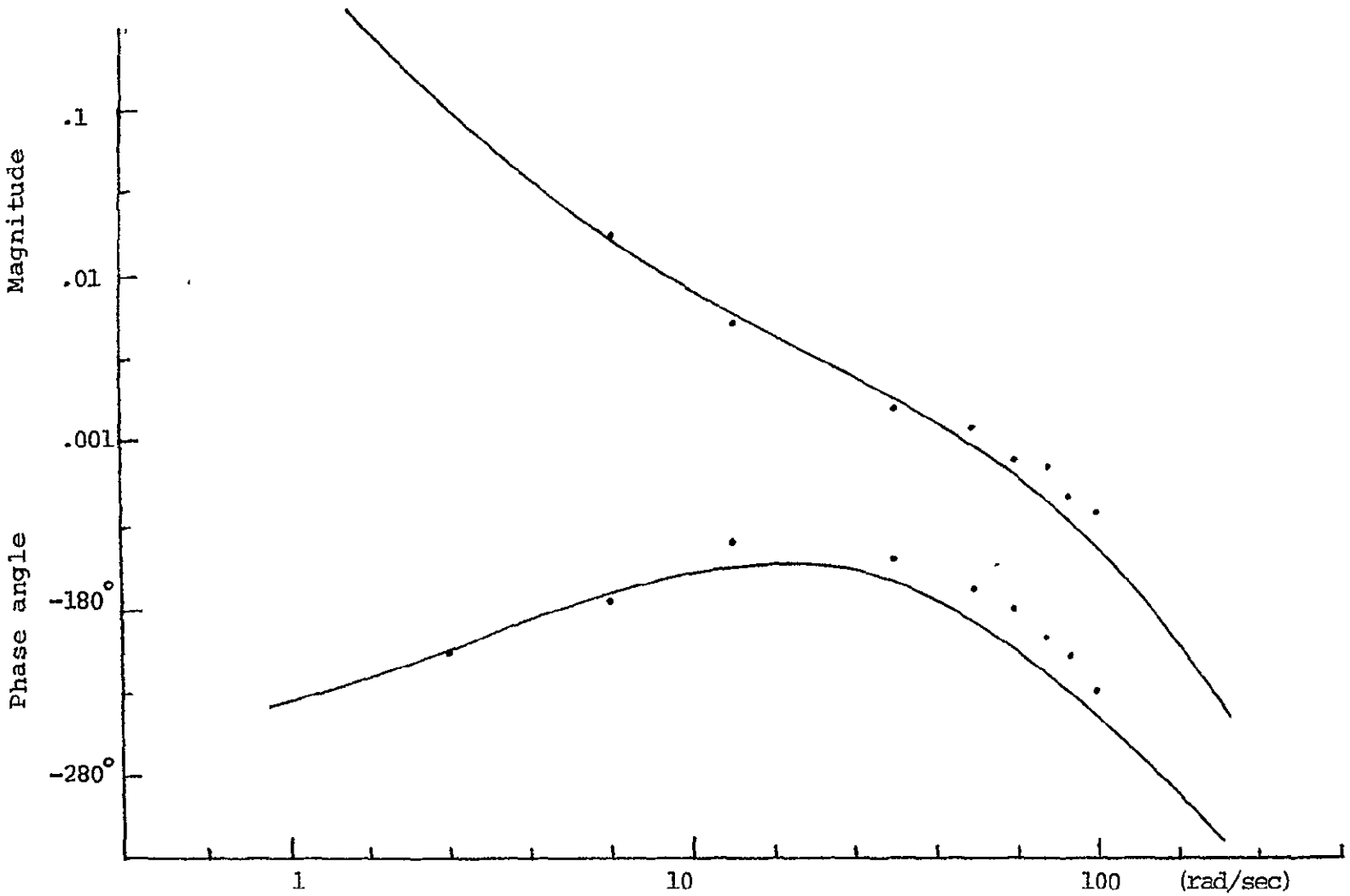
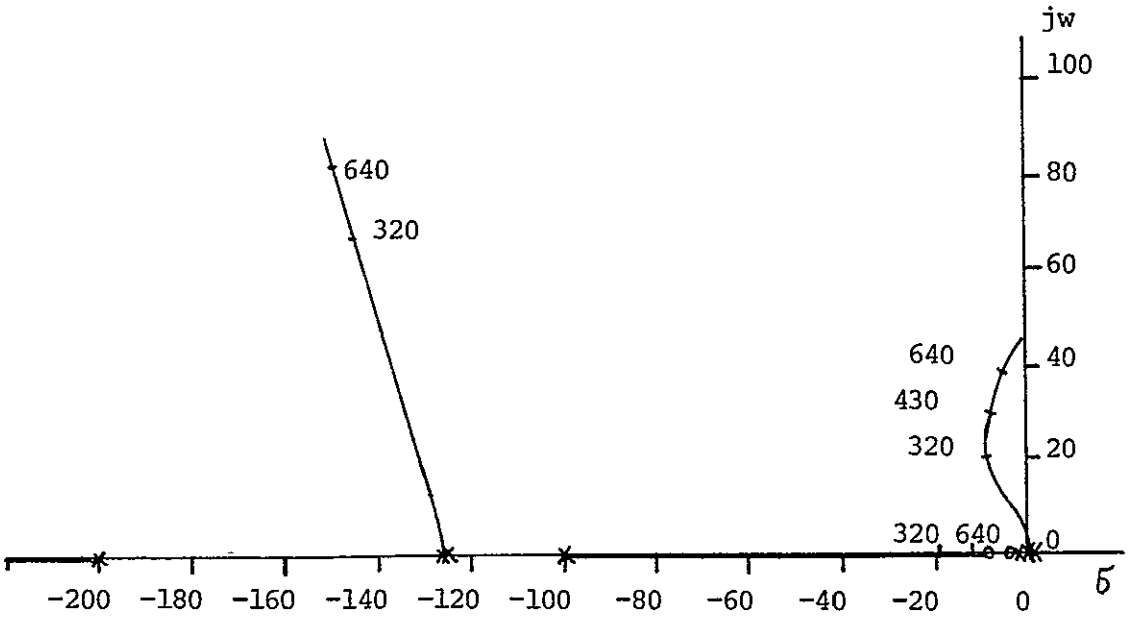
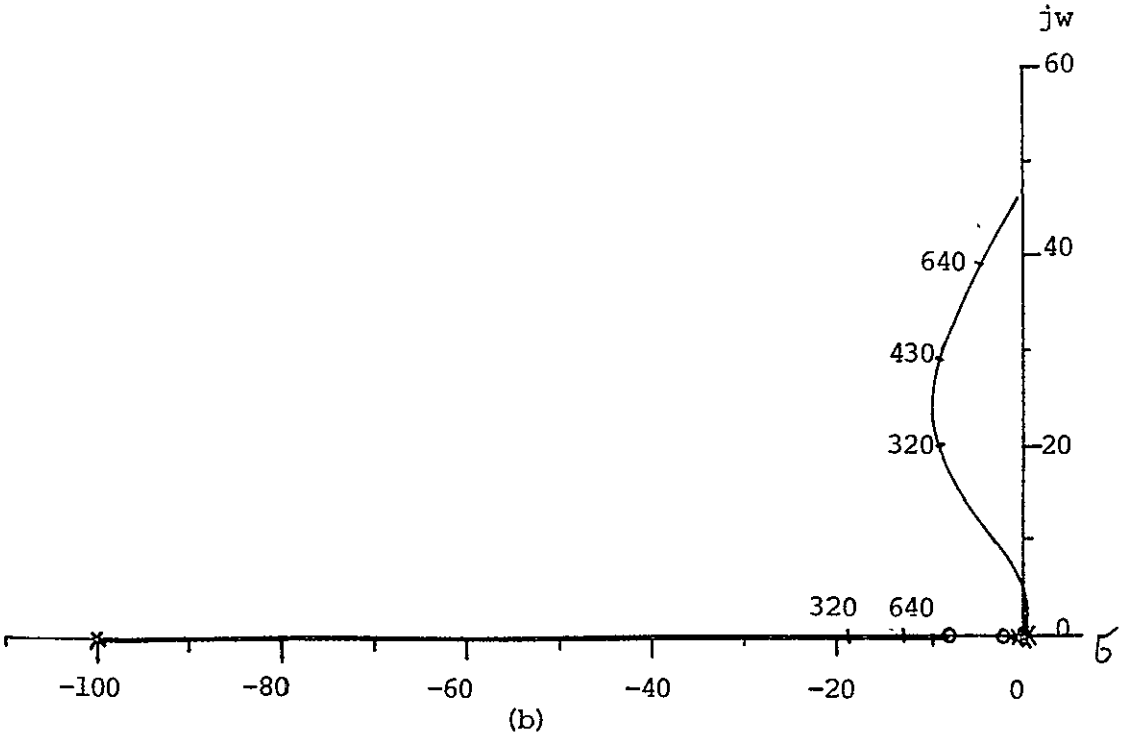


Figure 18

Drag degree of freedom open-loop Bode plot, 2/3



(a)



(b)

Figure 19

Root locus for drag degree of freedom

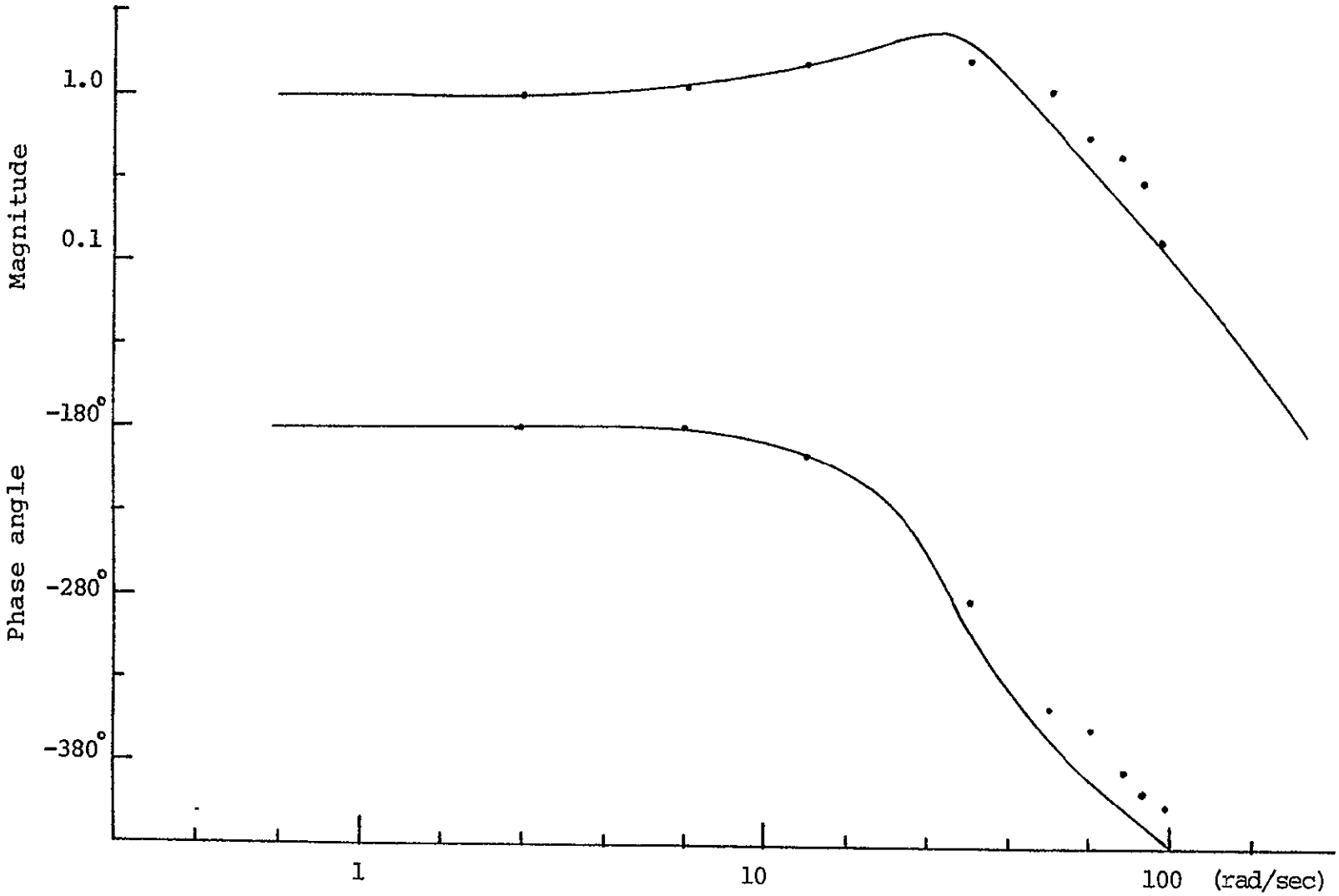


Figure 20

Drag degree of freedom closed-loop Bode lot, 2/1

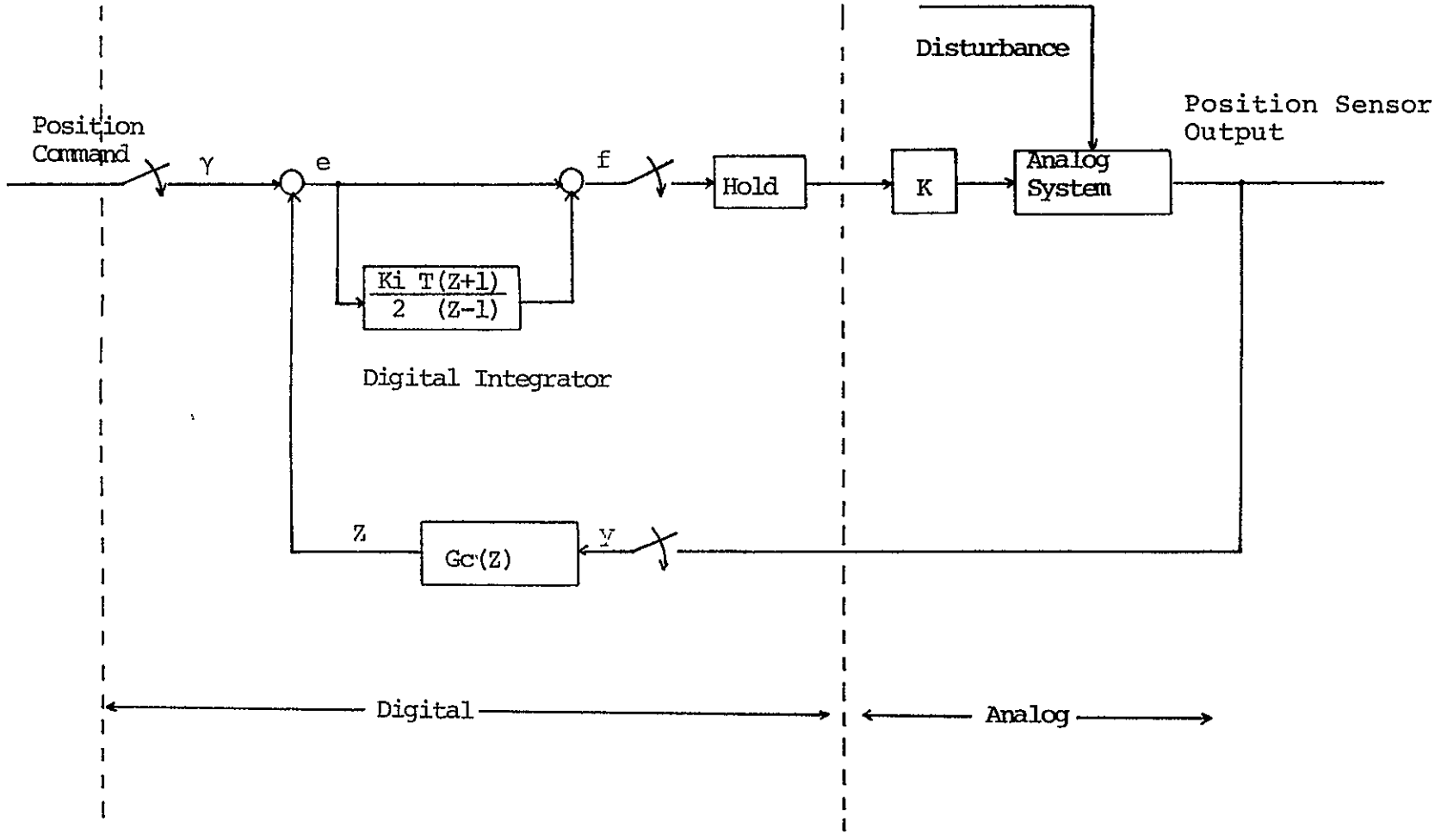
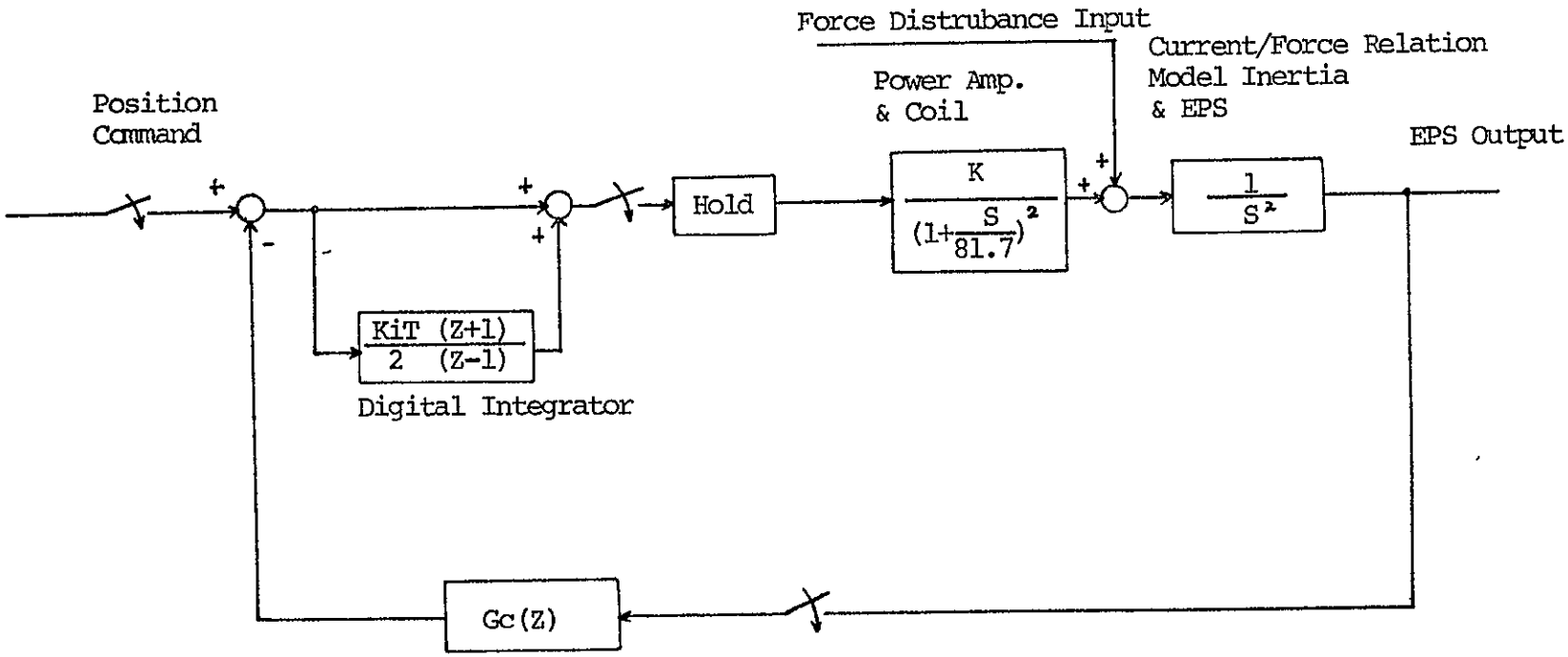


Figure 21
Sampled data analysis



$$Gc(z) = \frac{8.0853\ (z-0.73555)\ (z-0.35455)}{(z-z_1)(z-\overline{z}_1)}$$

$$z_1 = -0.11012 + 0.38434j$$

Figure 22 Lift degree of freedom sampled data analysis

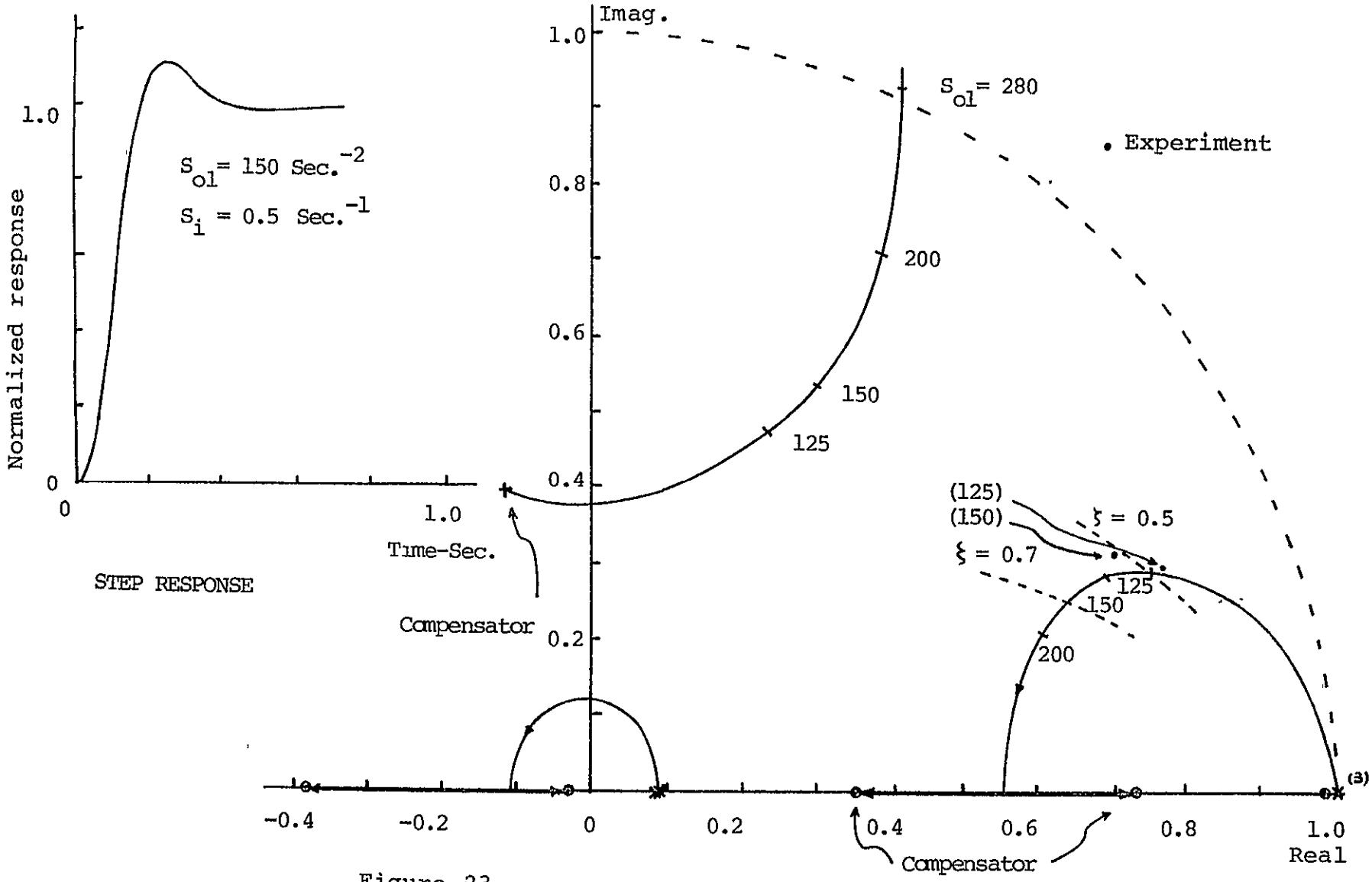


Figure 23

Lift degree of freedom Z-plane root locus and step response

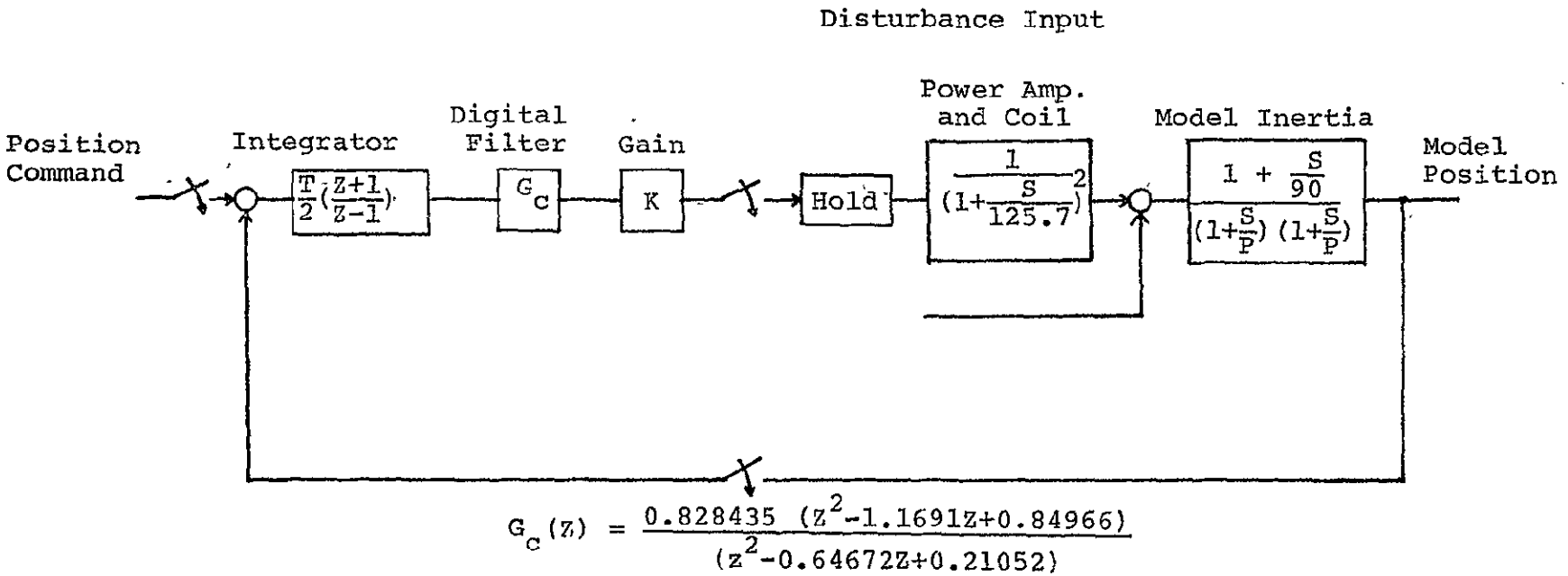


Figure 24 Pitch axis sampled data analysis

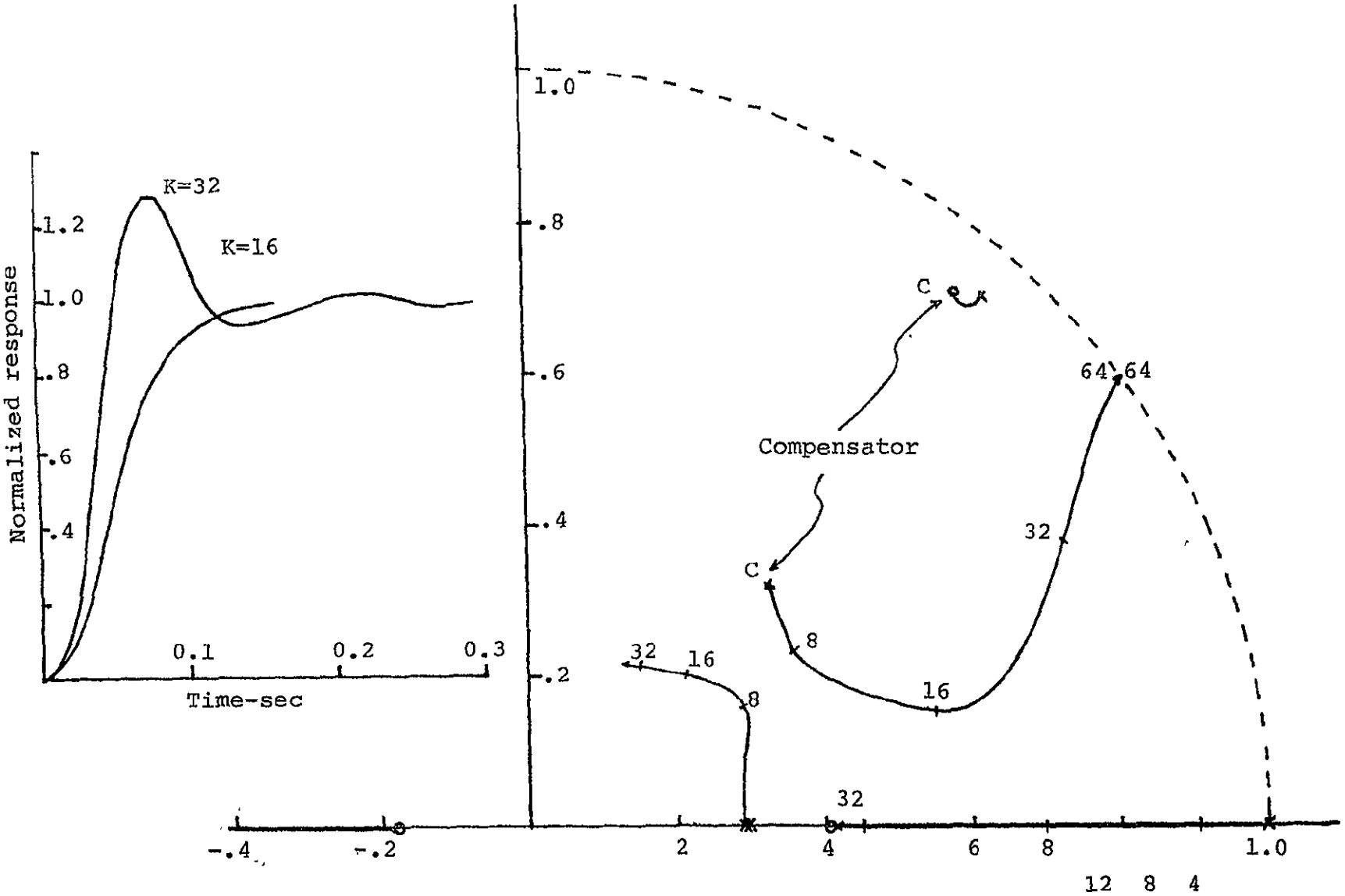


Figure 25 Pitch axis Z-plane root locus and step response

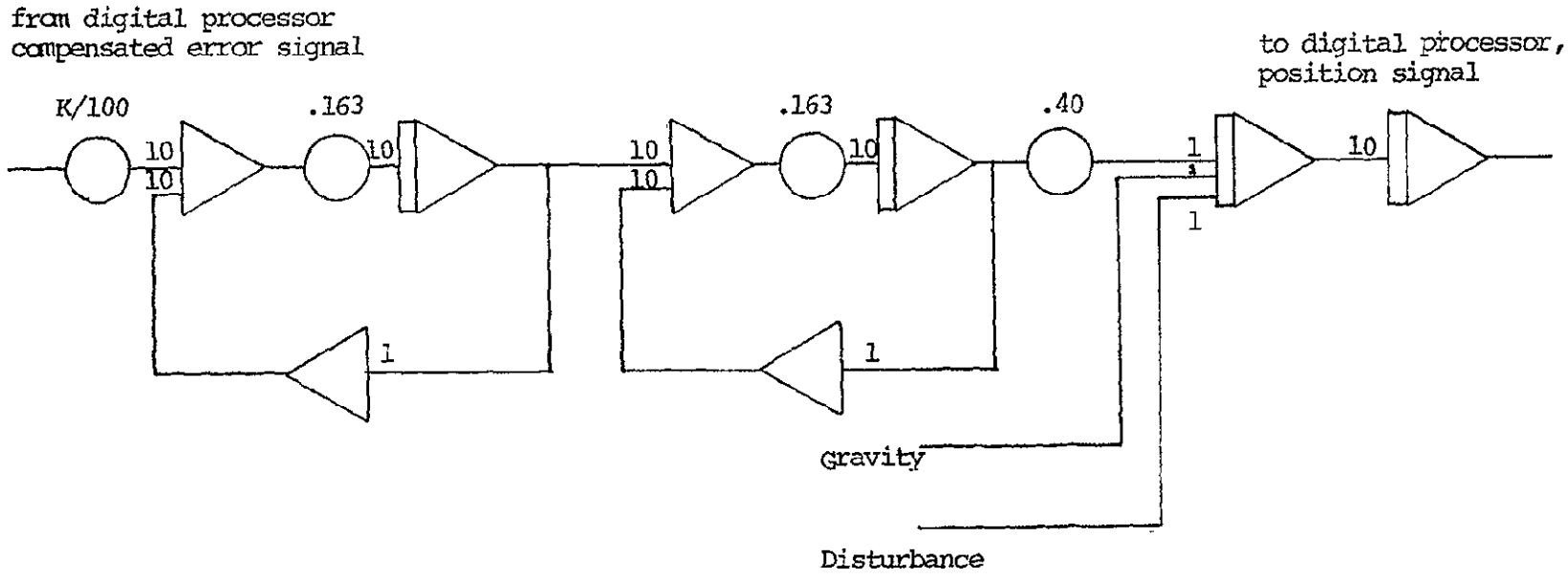


Figure 26

Lift degree of freedom hybrid simulation, analog computer system, time factor = 5

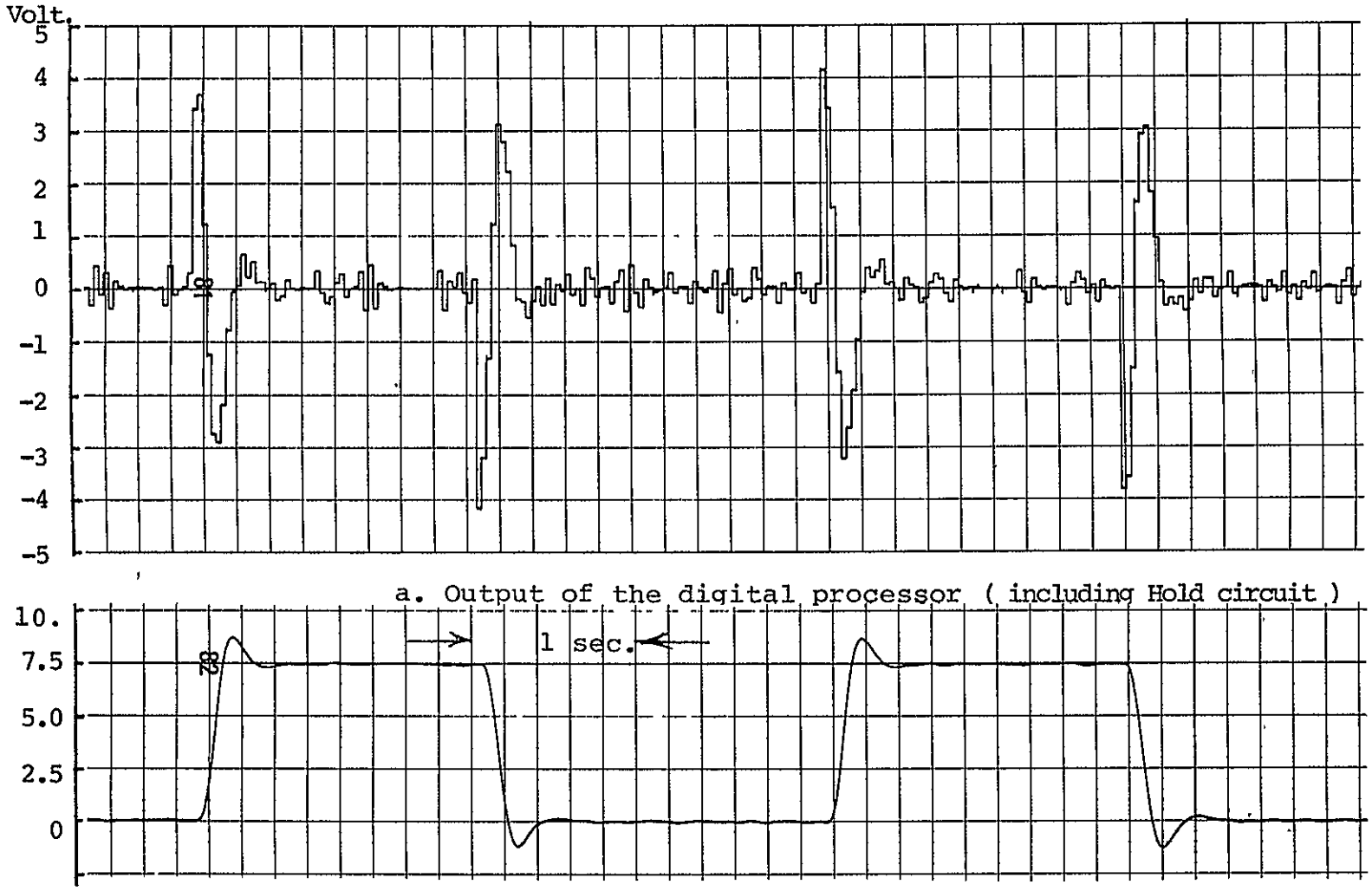
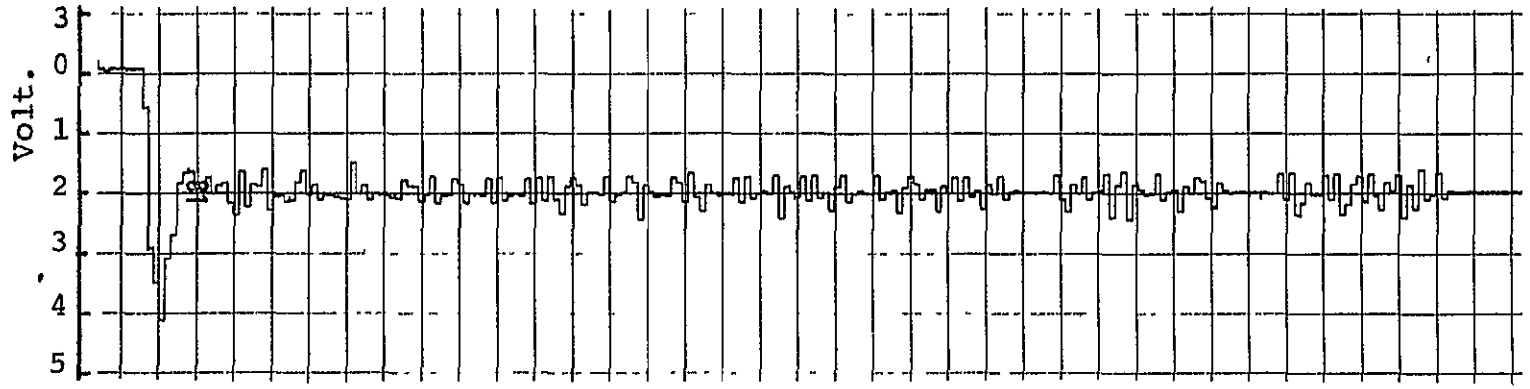
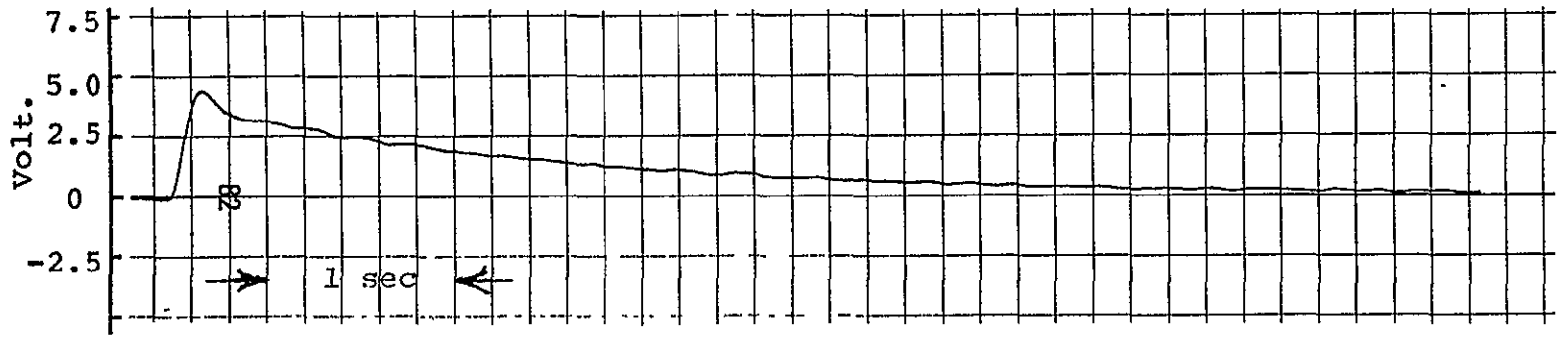


Figure 27 Lift degree of freedom response to step position commands
K=150, K_i=0.5



a. Output of the digital processor (including Hold circuit)



b. Output of the hybrid system, model position

Figure 28 Lift degree of freedom step response to a force disturbance input

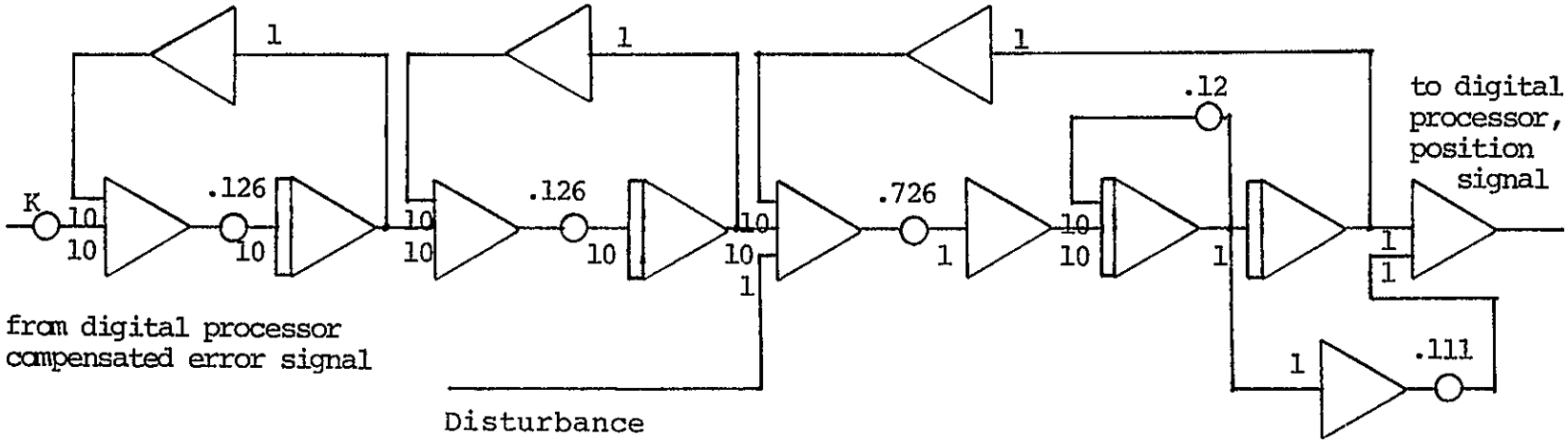
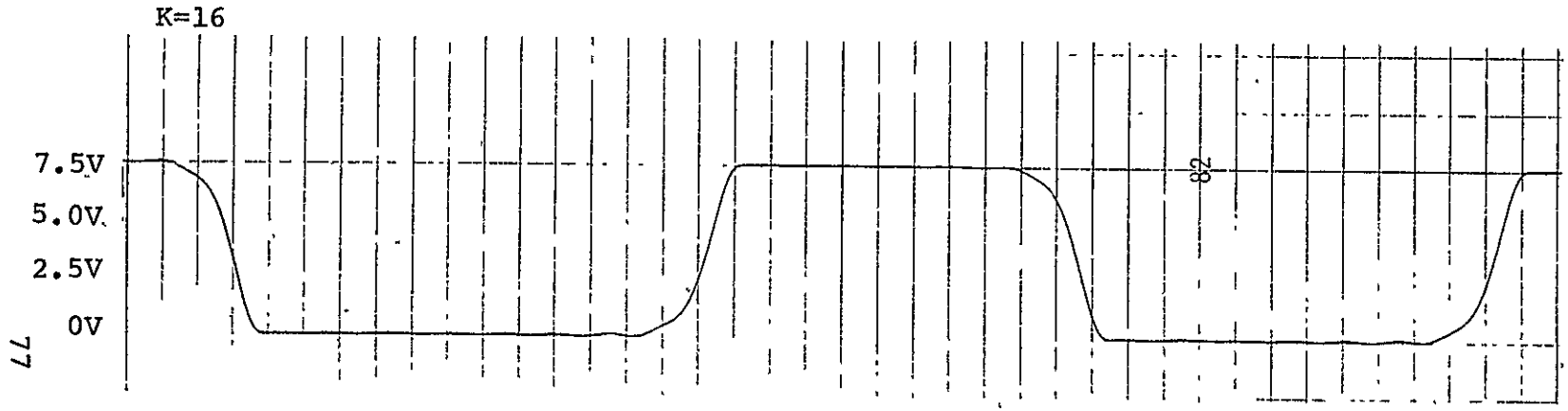
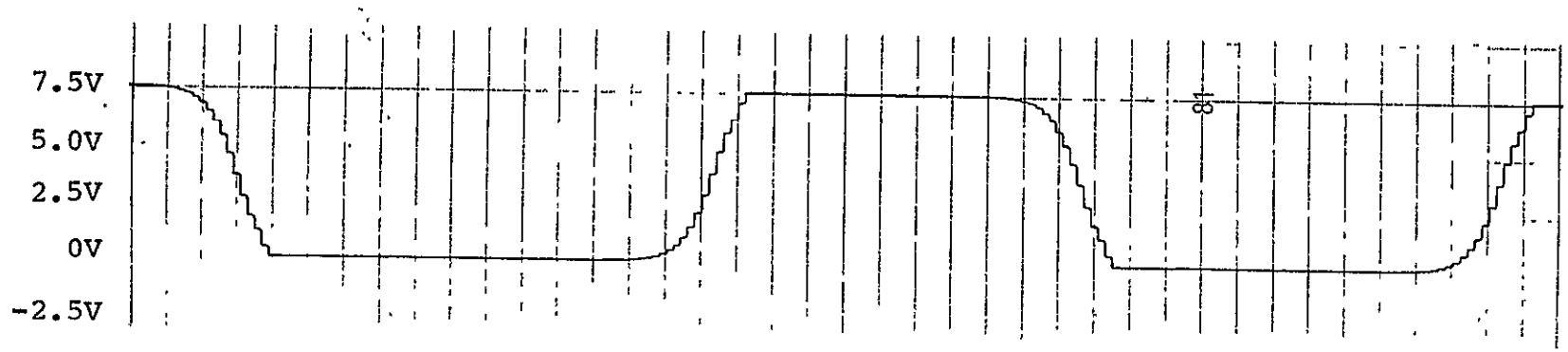


Figure 29

Pitch axis hybrid simulation, analog system,
time factor = 10

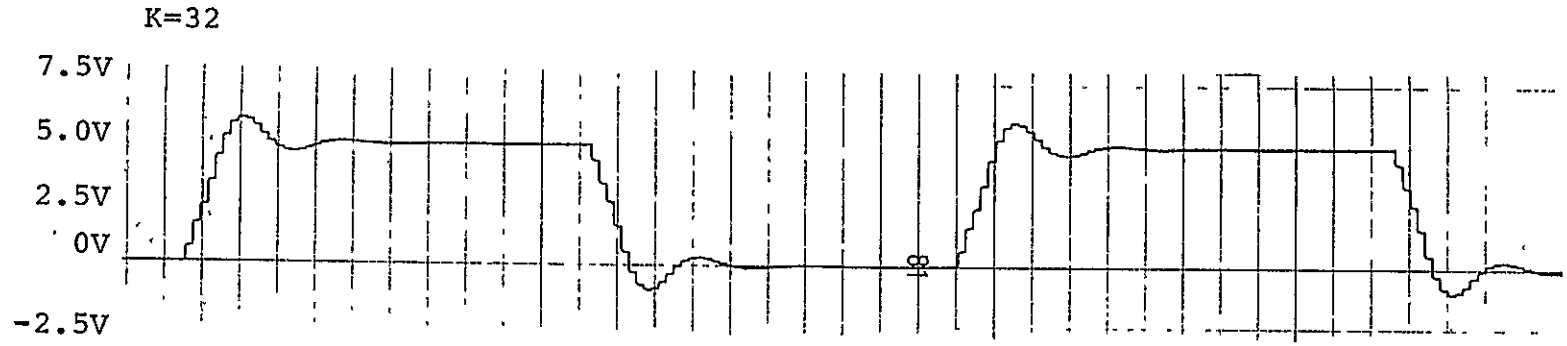


Output of the digital processor



Output of the analog system, model position

Figure 30a Hybrid simulation of the pitch degree of freedom. Step response, K=16



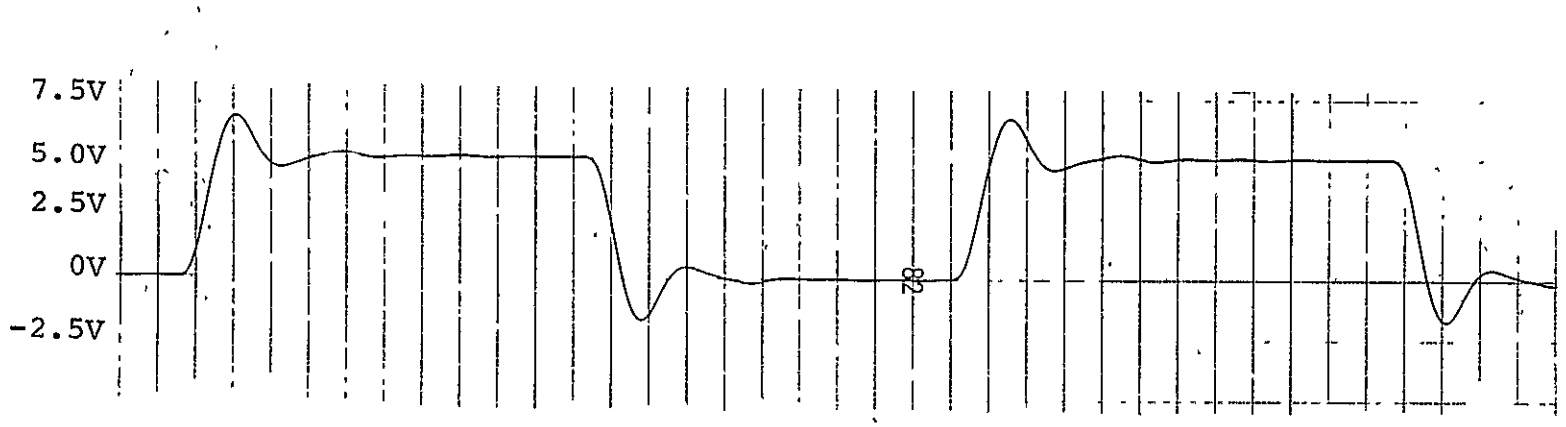


Figure 30b Hybrid simulation of the pitch degree of freedom. Step response, K=32

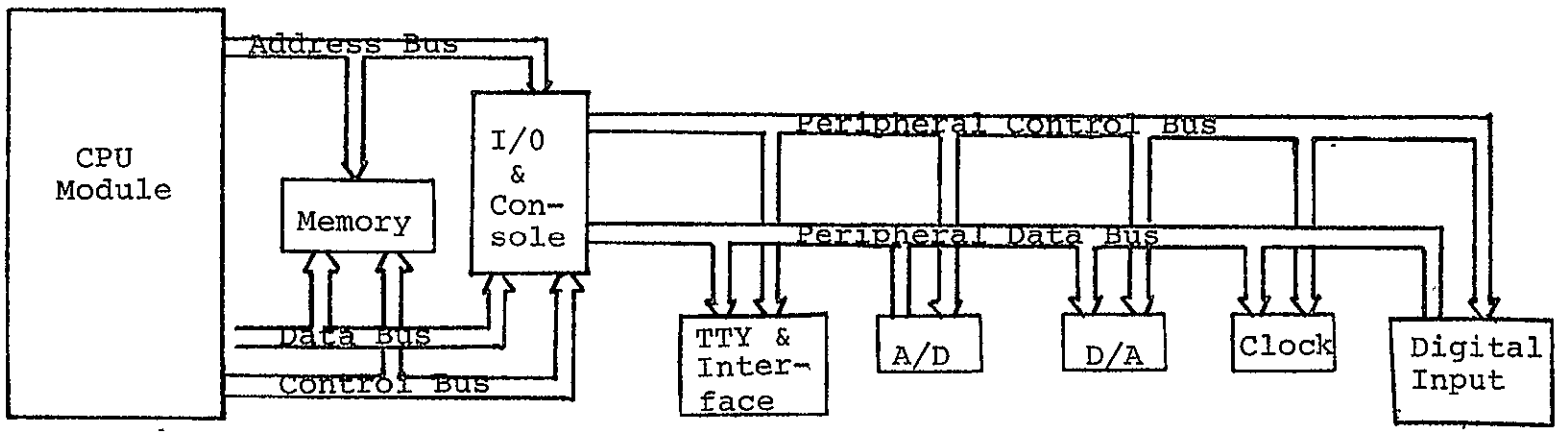


Figure 31. Block diagram of the microcomputer

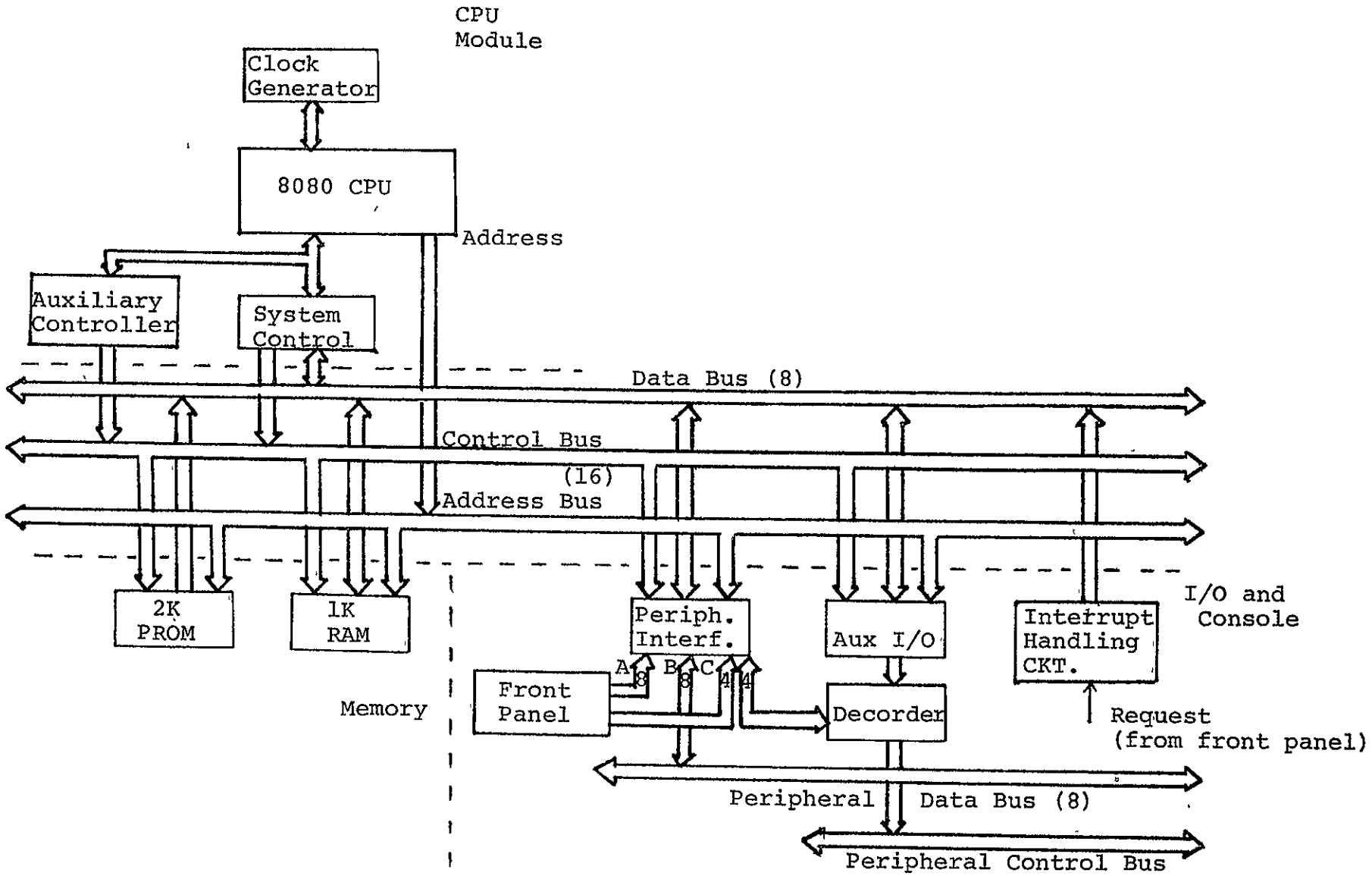
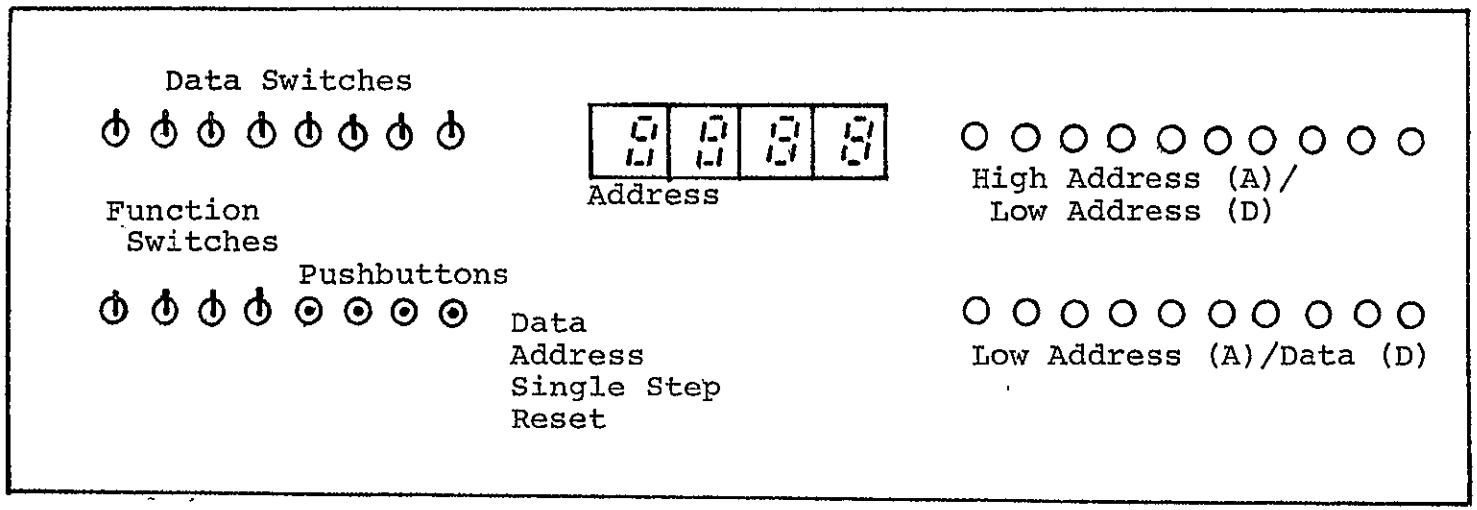


Figure 32 Schematic of the computer body



12 Toggle Switches
4 Pushbuttons
4 Seven-segment Displays
20 Leds

Figure 33 Schematic of Front Panel

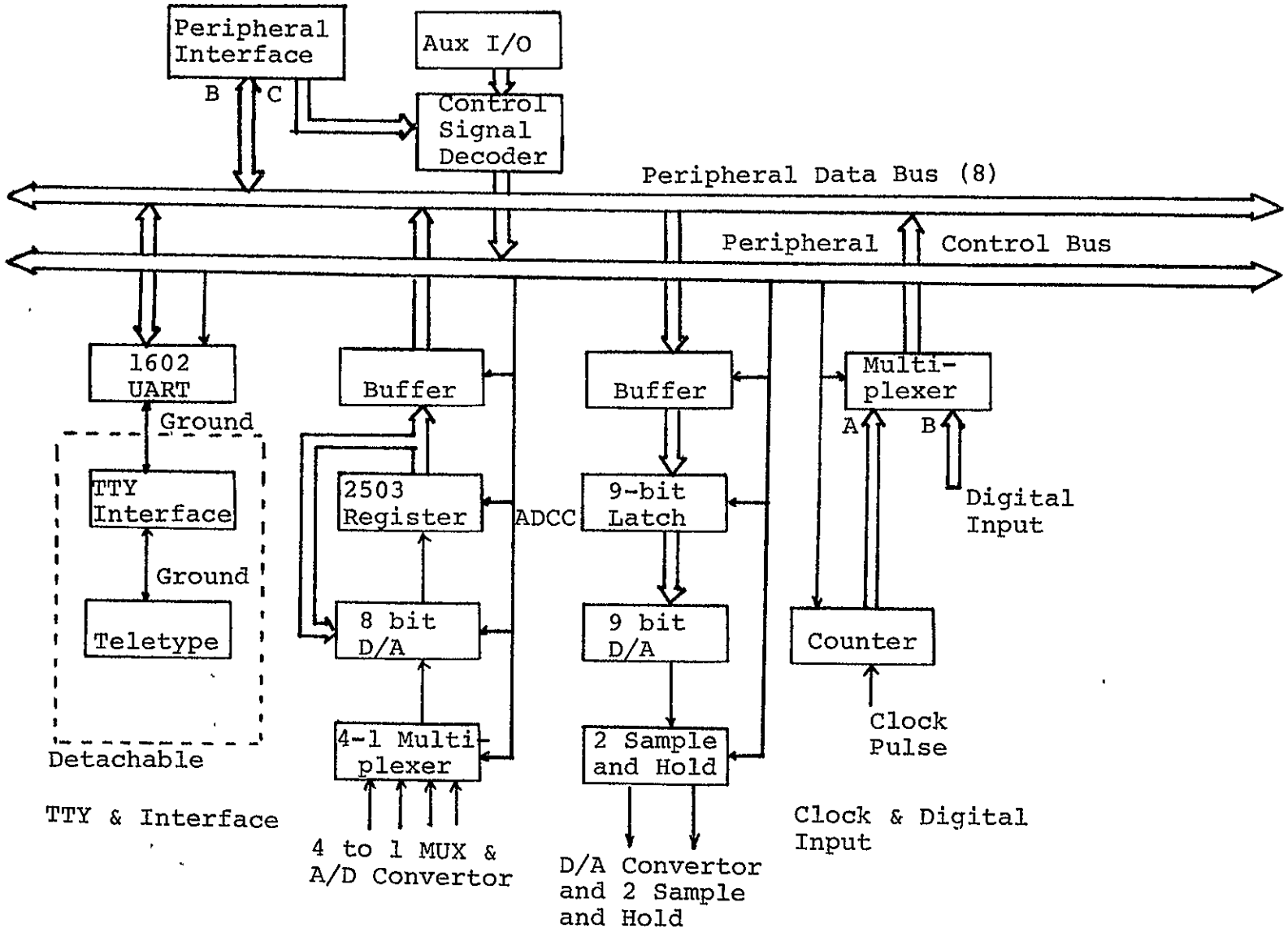


Figure 34 Schematic of peripherals

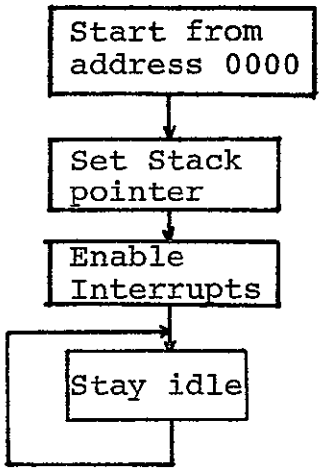


Figure 35

CONSOLE MONITOR (I) RESET

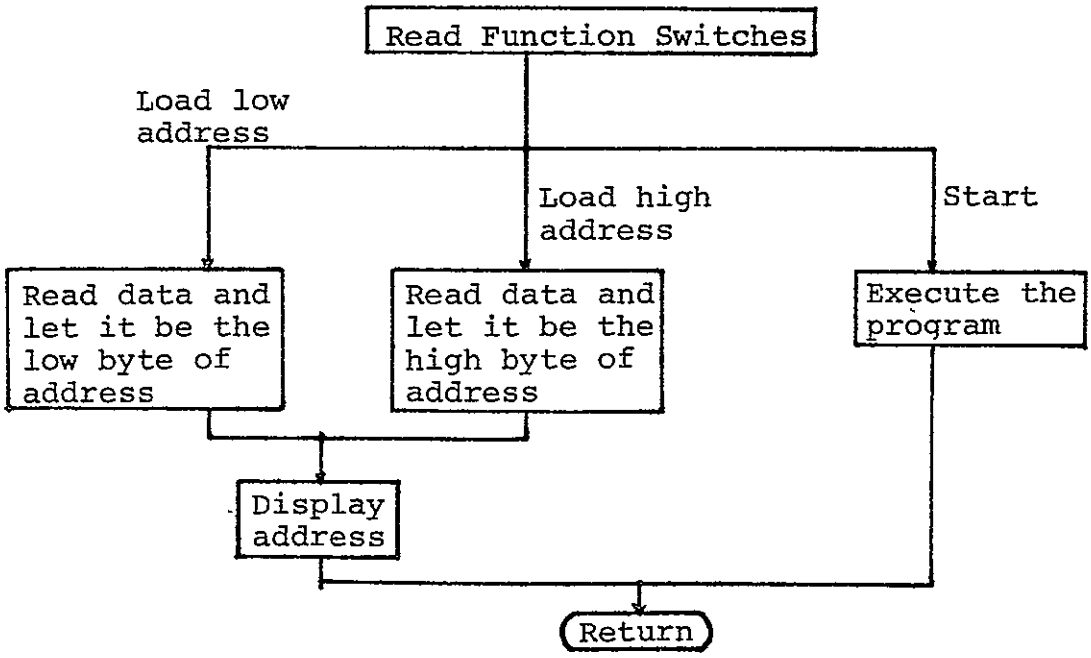


Figure 36

CONSOLE MONITOR (II) INTERRUPT (ADDRESS)

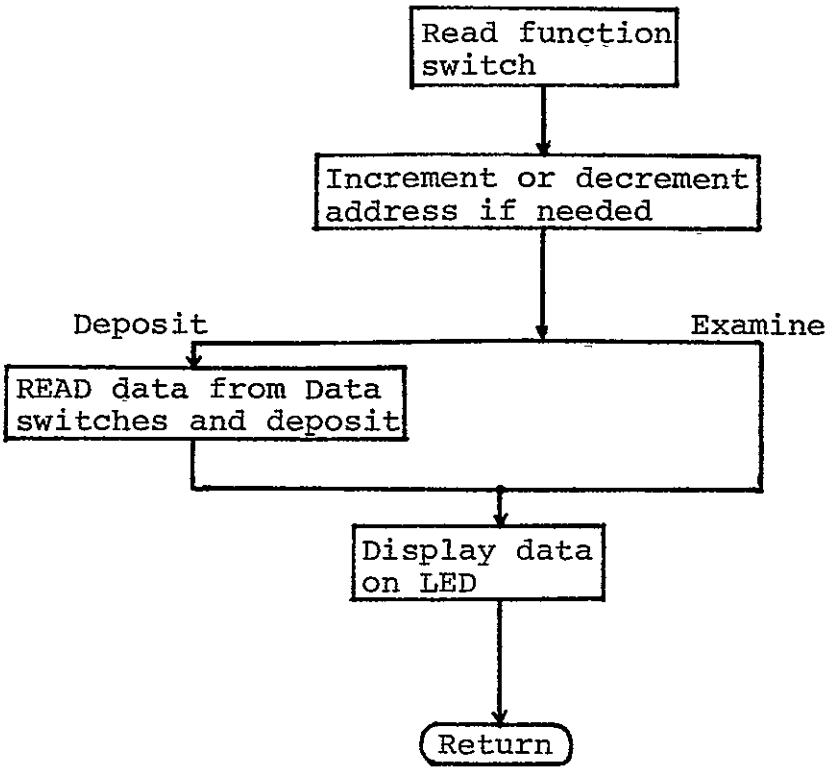


Figure 37

CONSOLE MONITOR (III) INTERRUPT (DATA)

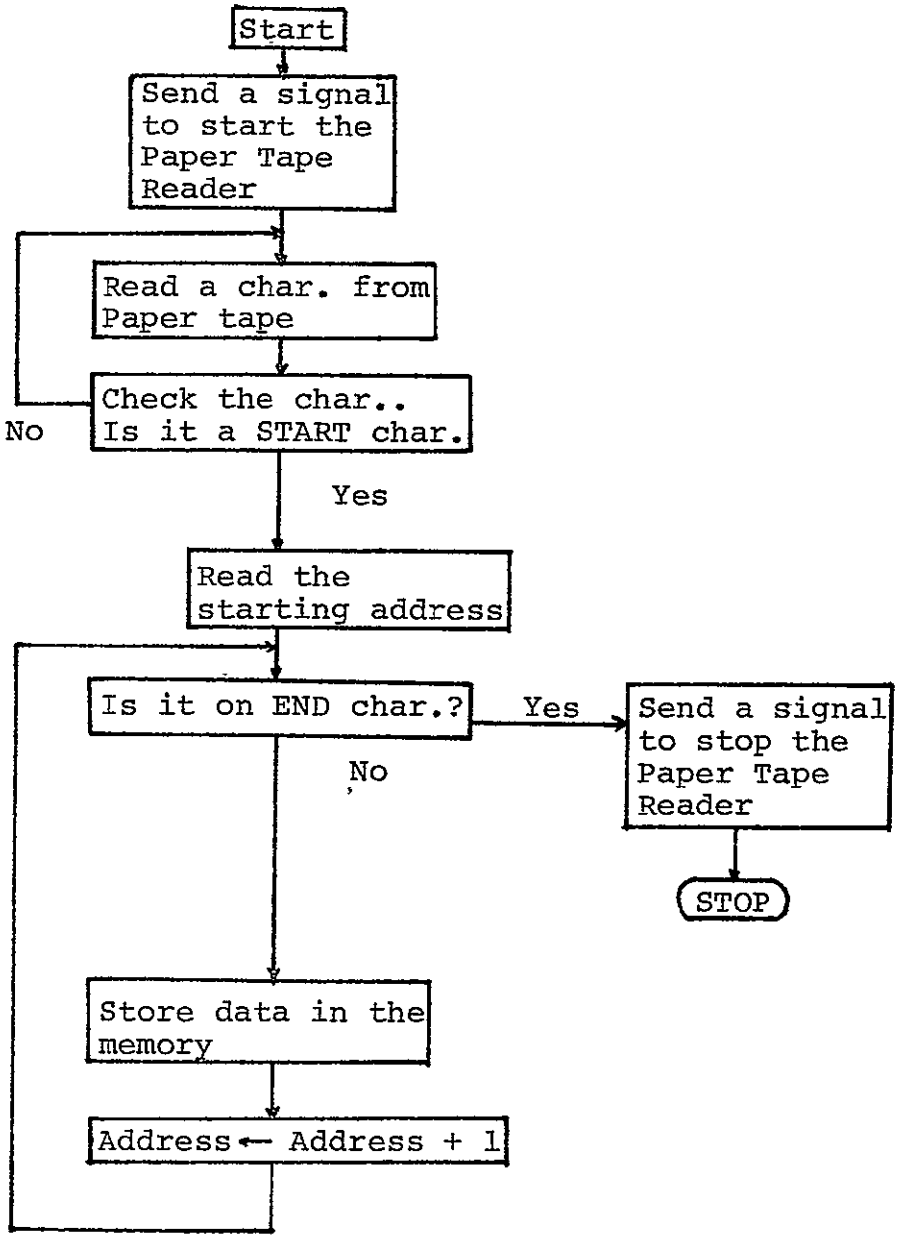


Figure 38

LOADER

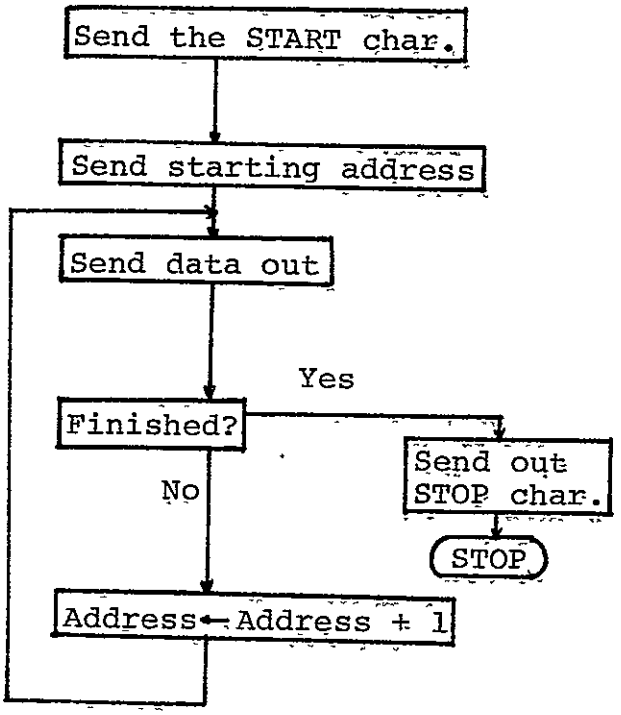


Figure 39

DUMPER

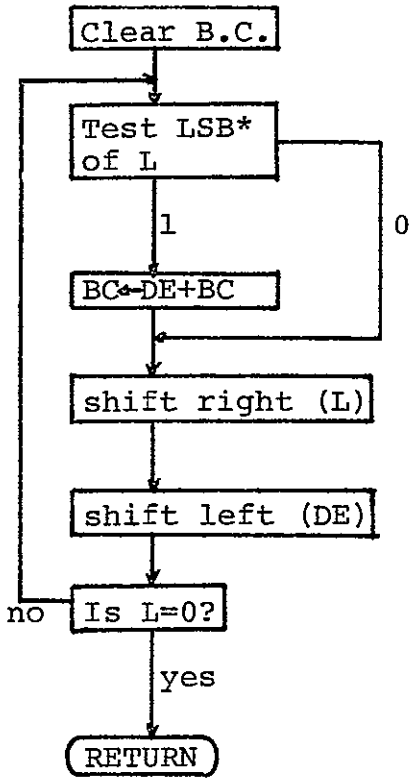


Figure 40

Flow chart for multiplication subroutine
BC ← DE * L

*LSB: least significant bit

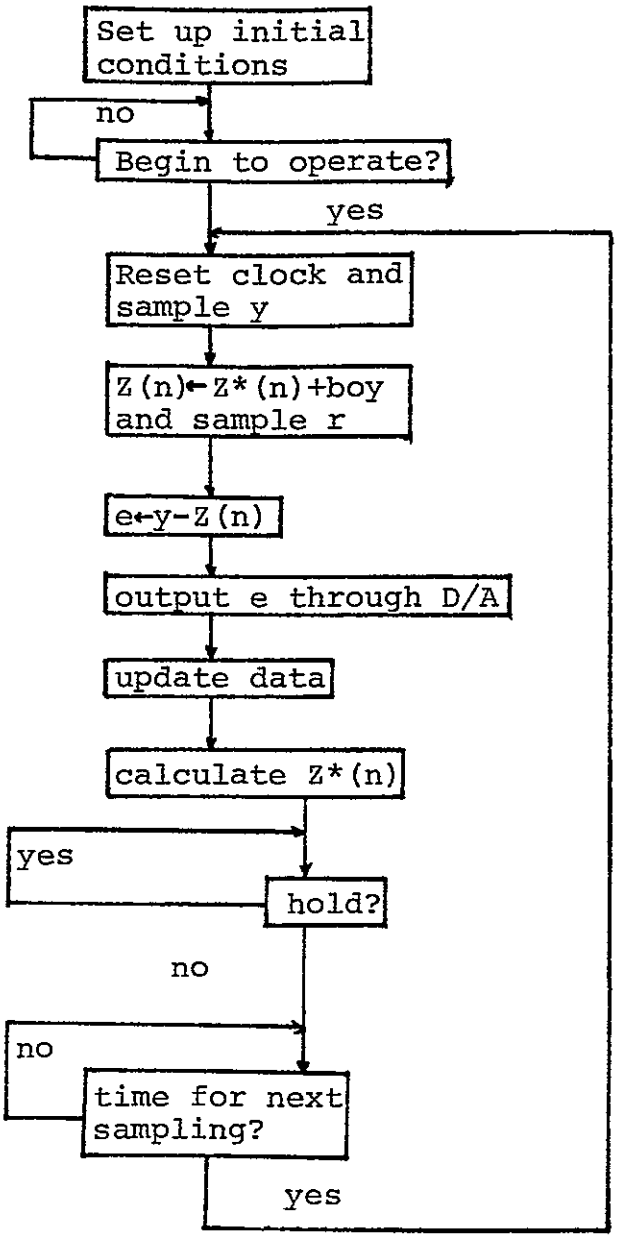


Figure 41 Flow chart of the control program

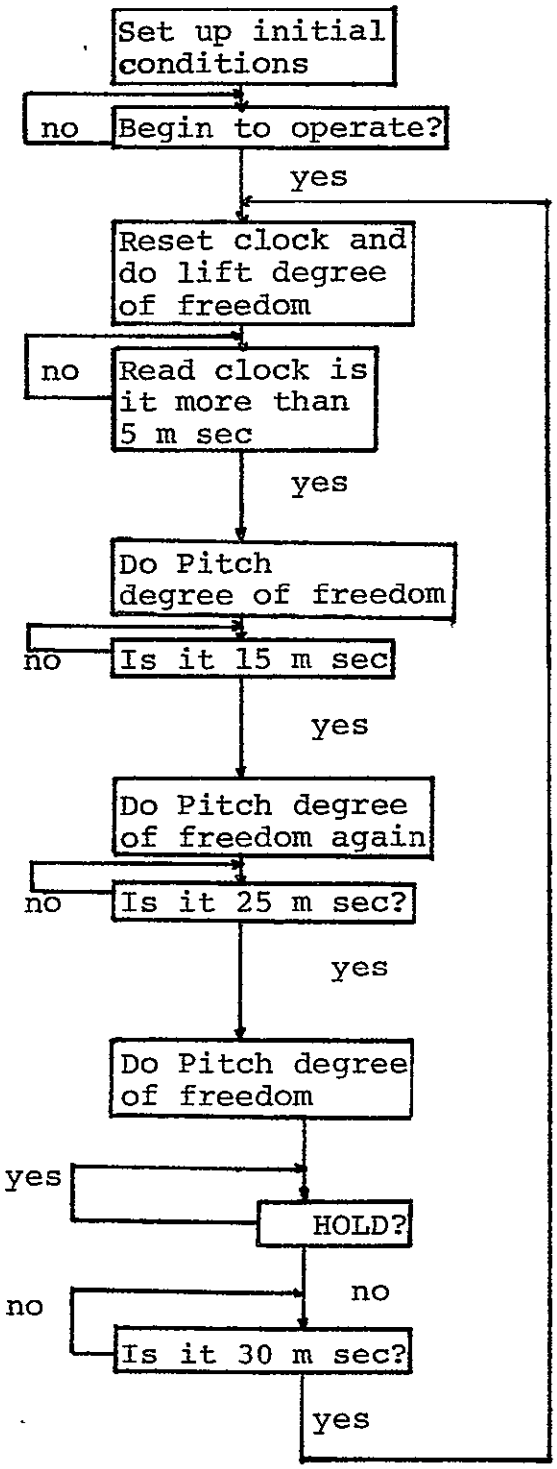


Figure 42 Scheduling of the microcomputer

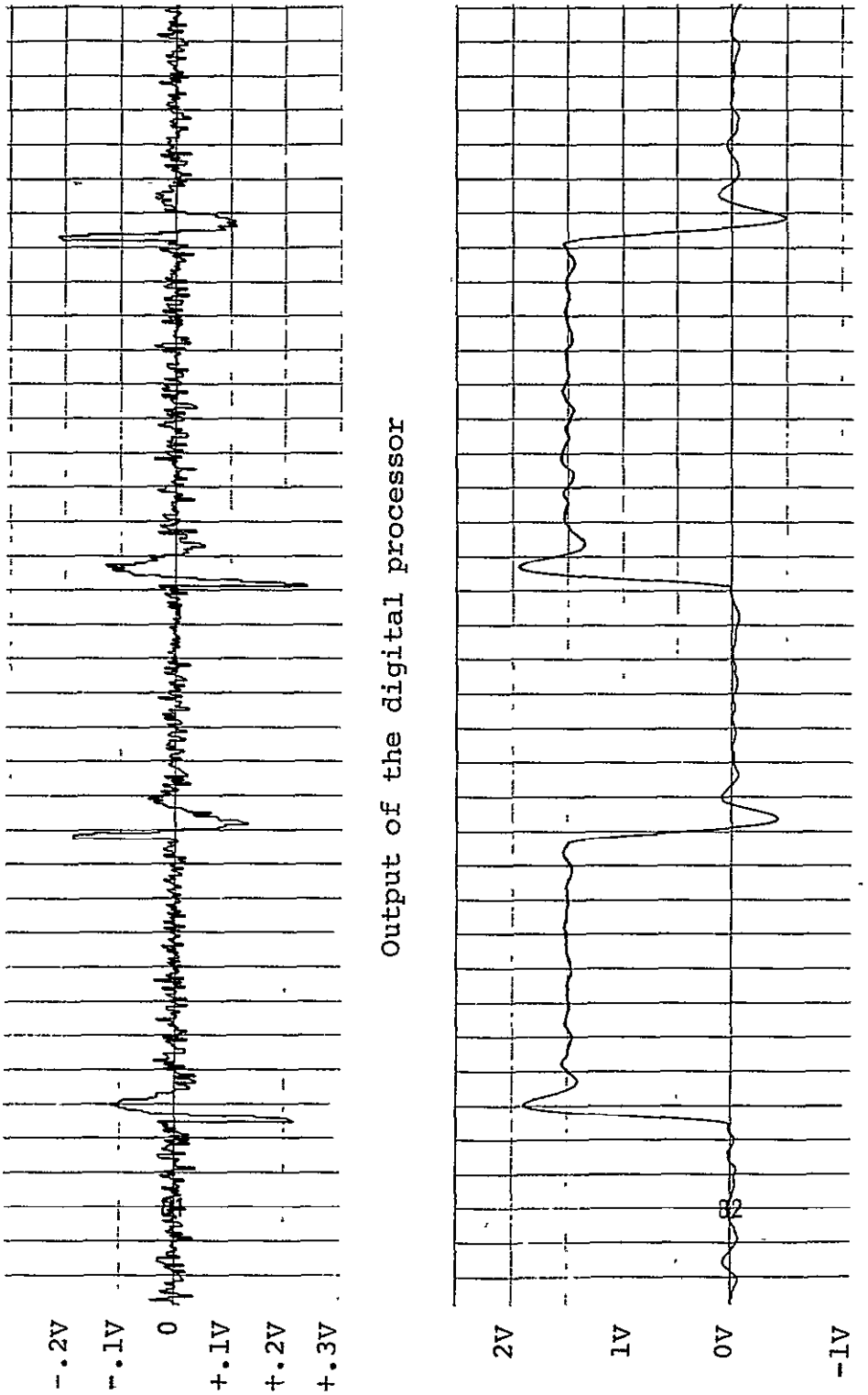


Figure 43 Microcomputer hybrid simulation of the lift degree of freedom. Step response, K=150, K_i=0

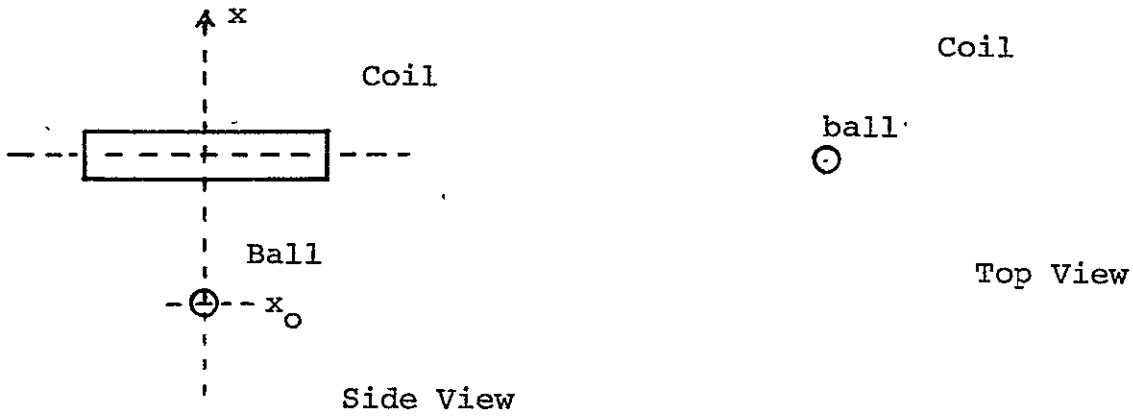


Figure 44 One-dimensional balance geometry

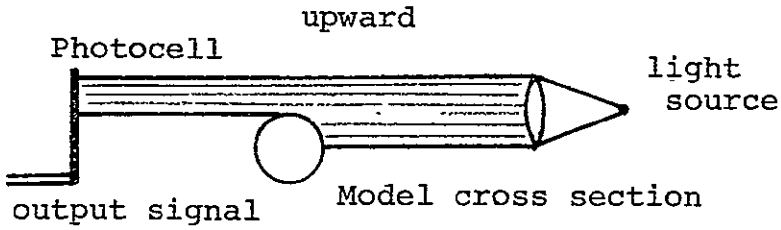


Figure 45 Columnating lens

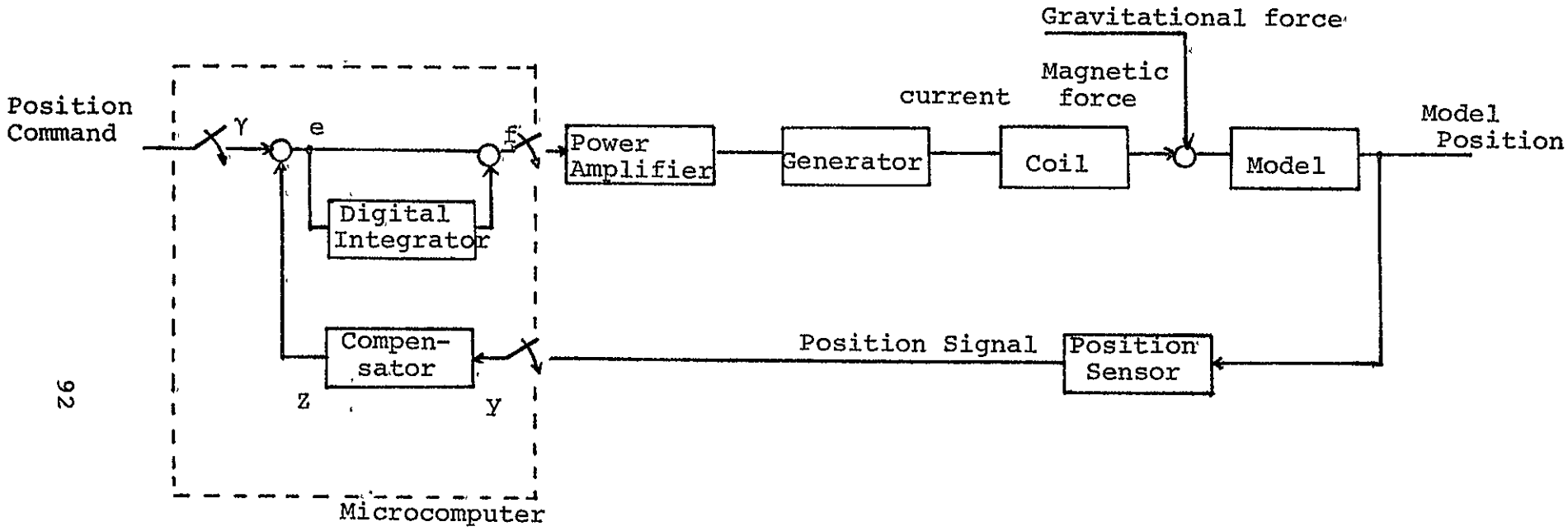


Figure 46 Block diagram of the one-dimensional balance system

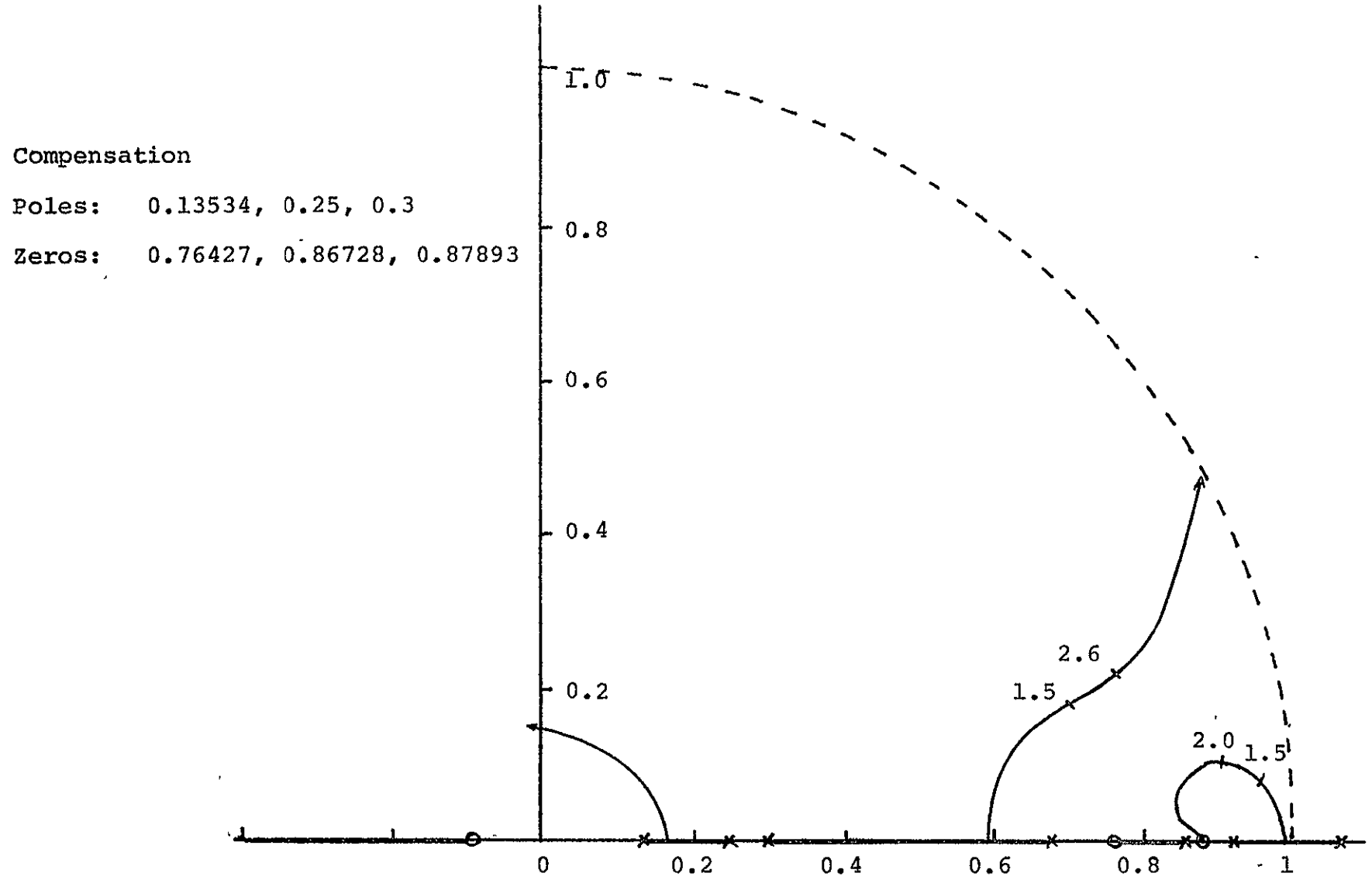


Figure 47 Z-plane root locus for 100 Hz sampling frequency digital compensator for one-dimensional balance

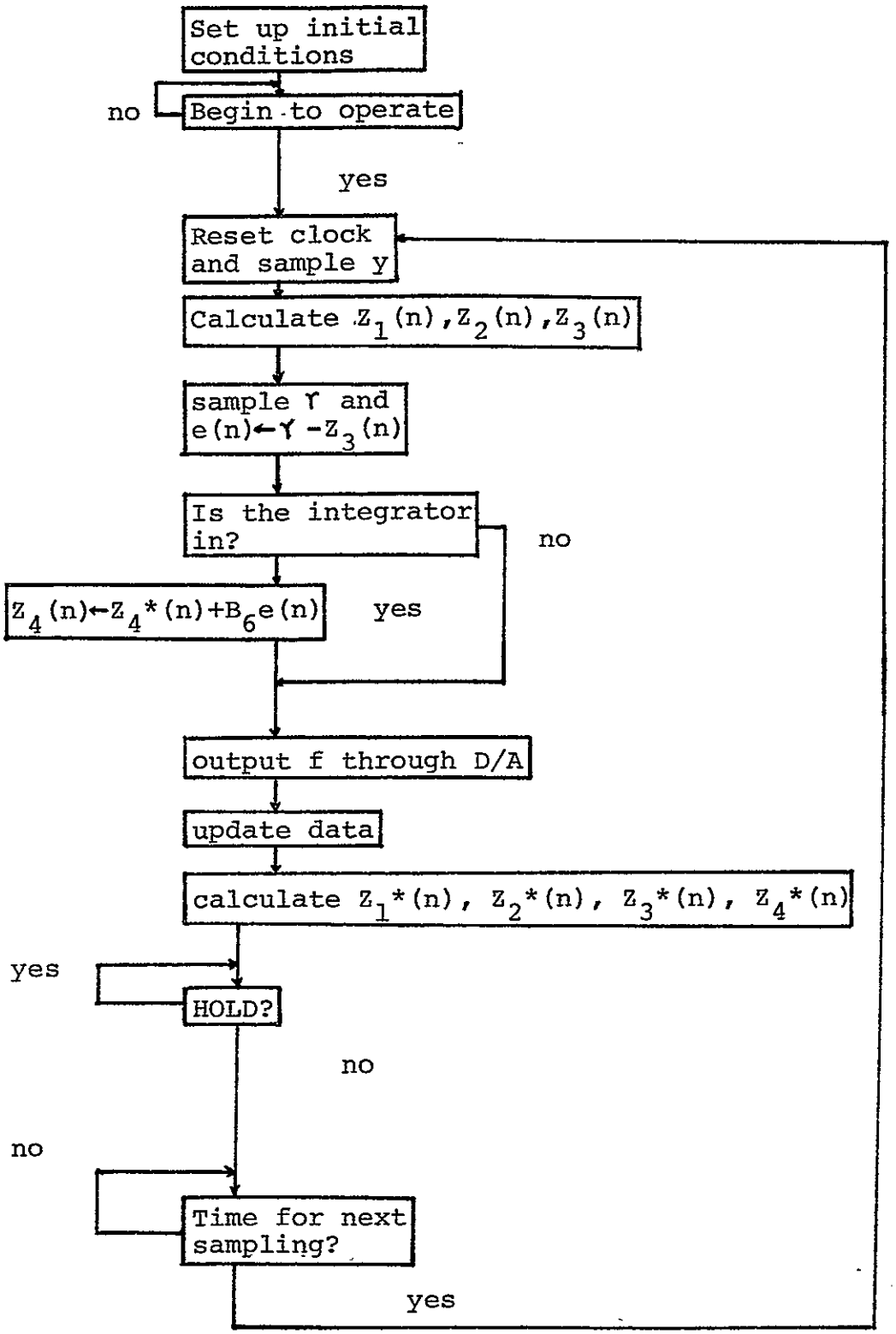


Figure 48 Flow chart of the program for the one-dimensional balance system

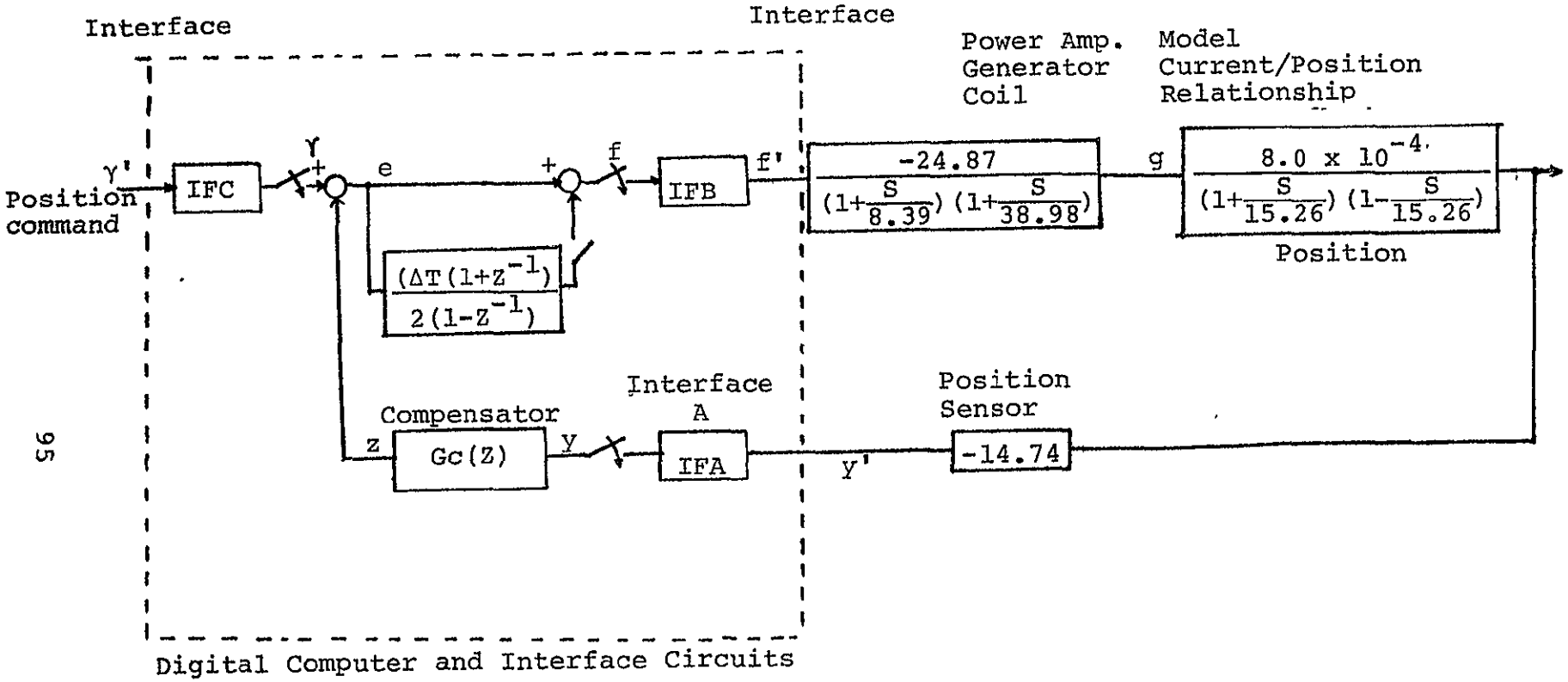
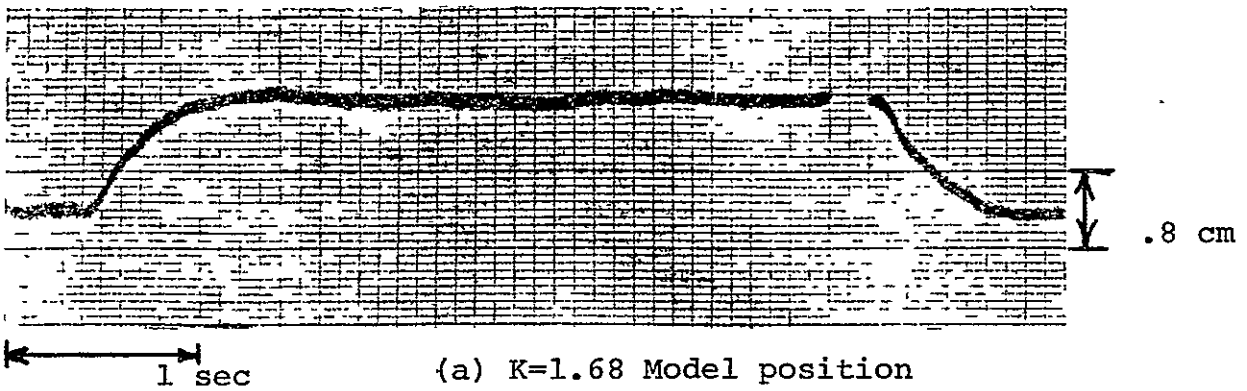
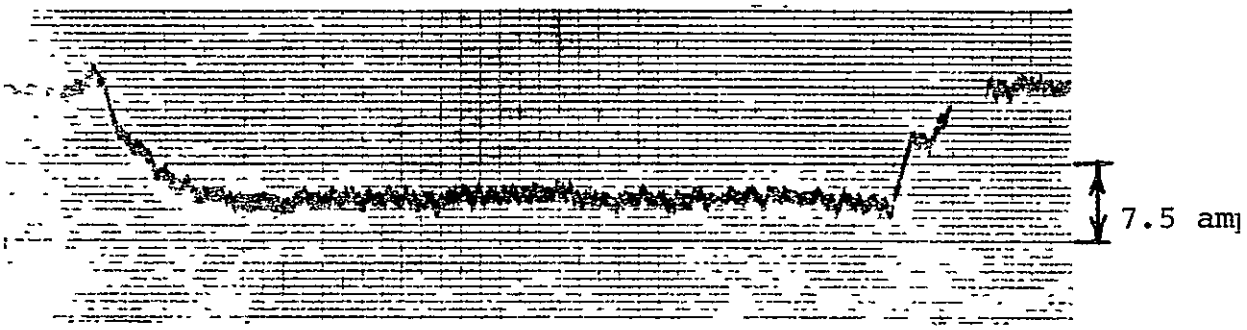


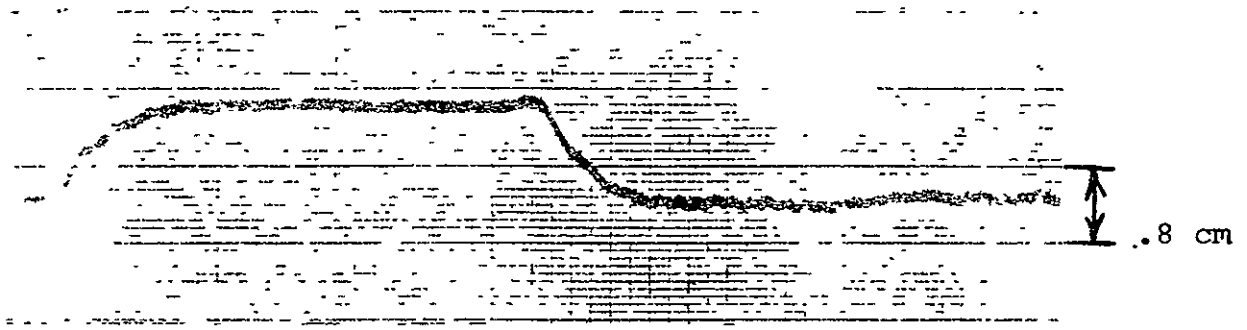
Figure 49 Schematic of the one-dimensional balance system, including interface circuits



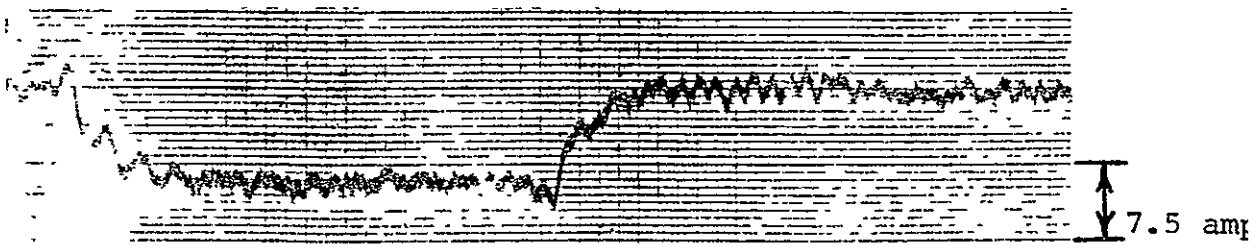
(a) K=1.68 Model position



(b) K=1.68 Current through the coil

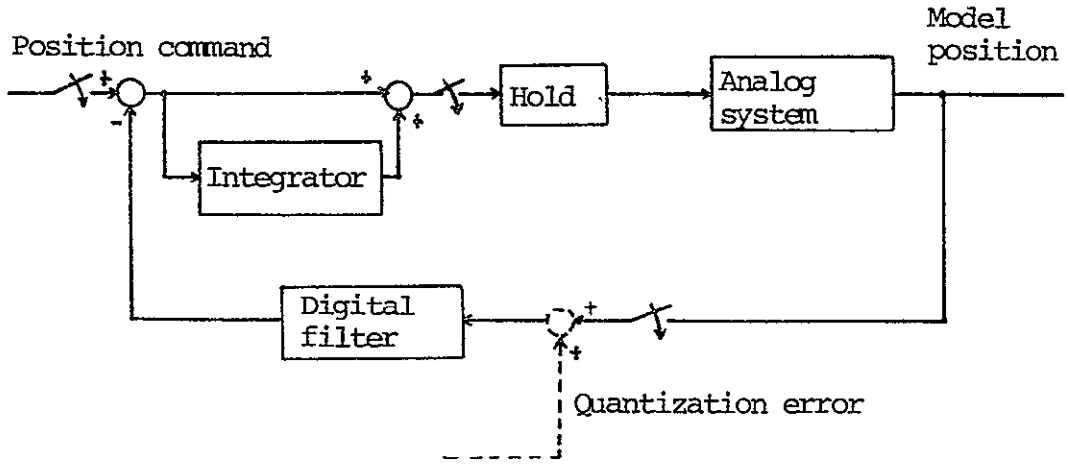


(c) K=1.92 Model position

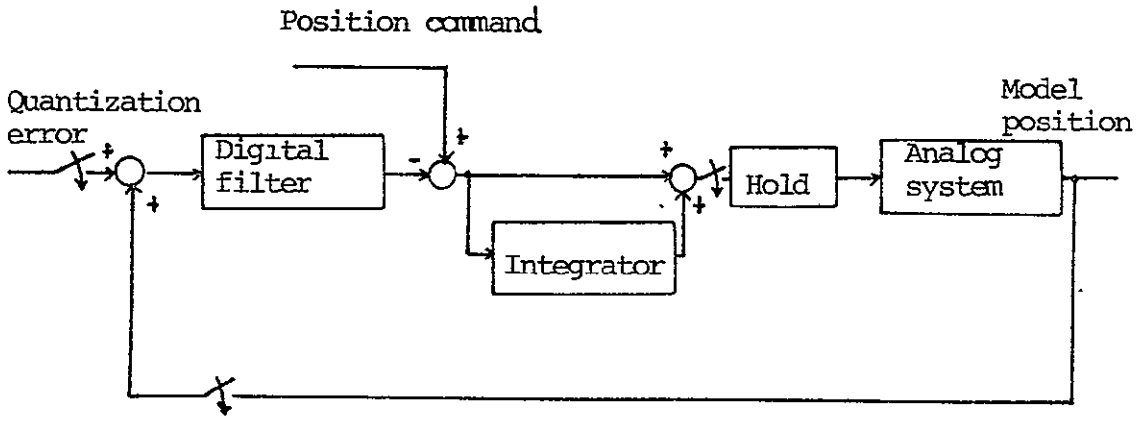


(d) K=1.92 Current through the coil

Figure 50 Step responses of the one dimensional balance system



(a)



(b)

Figure 51
Analysis of quantization error

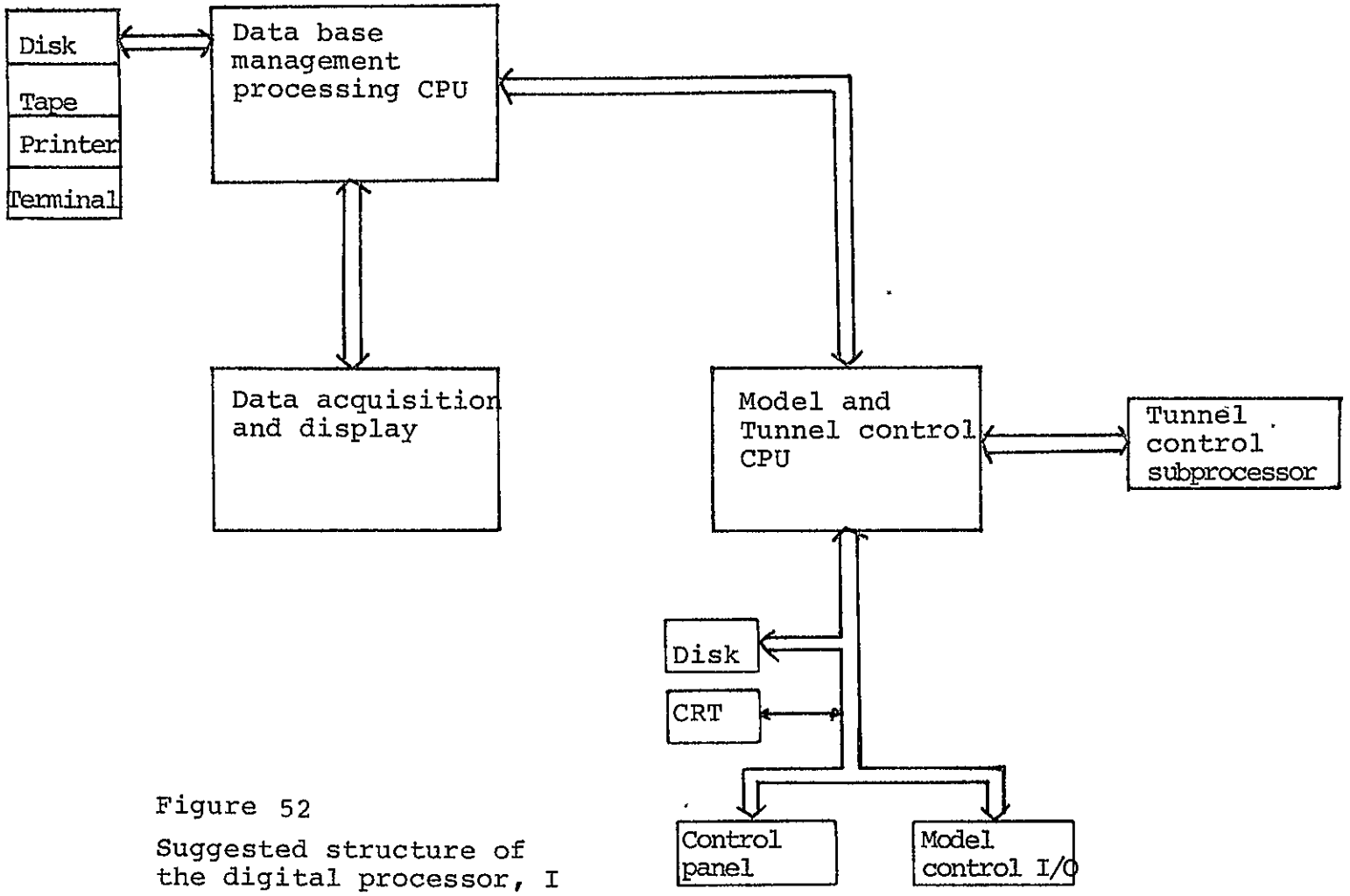


Figure 52

Suggested structure of the digital processor, I

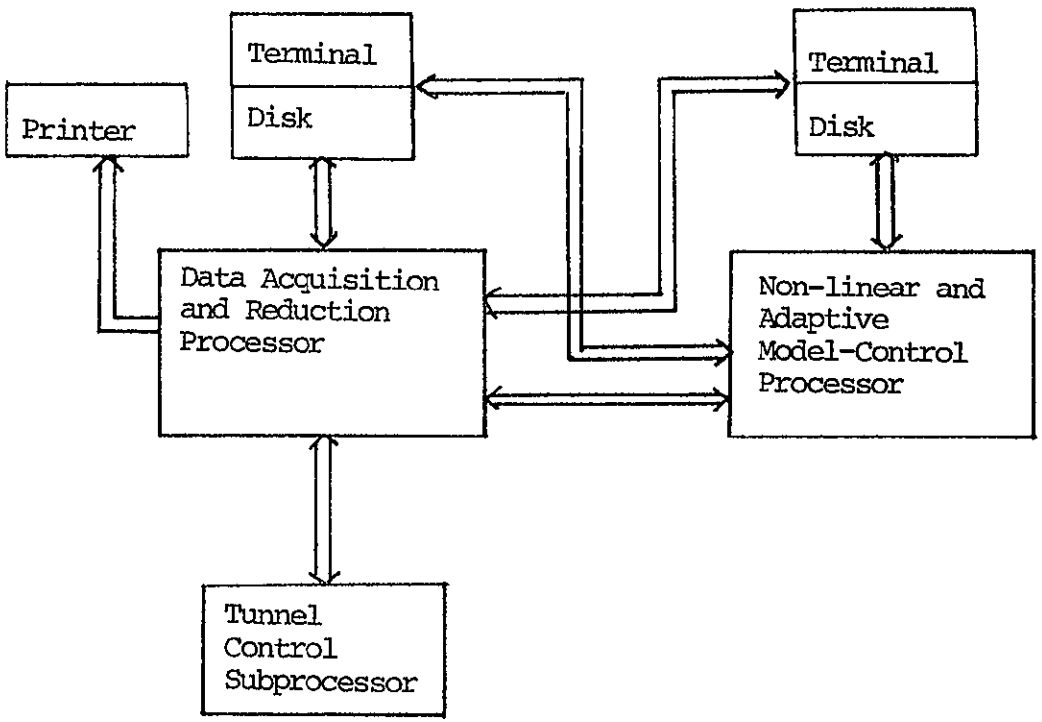


Figure 53

Suggested structure of the digital processor, II

Appendix A. INSTRUCTION LIST FOR INTEL 8080 MICROCOMPUTER

JUMP

C3	JMP	Adr
C2	JNZ	Adr
CA	JZ	Adr
D2	JNC	Adr
DA	JC	Adr
E2	JPO	Adr
EA	JPE	Adr
F2	JP	Adr
FA	JM	Adr
E9	PCHL	

CALL

CD	CALL	Adr
C4	CNZ	Adr
CC	CZ	Adr
D4	CNC	Adr
DC	CC	Adr
E4	CPO	Adr
EC	CPE	Adr
F4	CP	Adr
FC	CM	Adr

RETURN

C9	RET	
C0	RNZ	
C8	RZ	
D0	RNC	
D8	RC	
E0	RPO	
E8	RPE	
F0	RP	
F8	RM	

RESTART

C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7

ROTATE†

07	RLC	
0F	RRC	
17	RAL	
1F	RAR	

CONTROL

00	NOP	
76	HLT	
F3	DI	
FB	EI	

MOVE (cont)

58	MOV	E,B	
59	MOV	E,C	
5A	MOV	E,D	
5B	MOV	E,E	
5C	MOV	E,H	
5D	MOV	E,L	
5E	MOV	E,M	
5F	MOV	E,A	
60	MOV	H,B	
61	MOV	H,C	
62	MOV	H,D	
63	MOV	H,E	
64	MOV	H,H	
65	MOV	H,L	
66	MOV	H,M	
67	MOV	H,A	
68	MOV	L,B	
69	MOV	L,C	
6A	MOV	L,D	
6B	MOV	L,E	
6C	MOV	L,H	
6D	MOV	L,L	
6E	MOV	L,M	
6F	MOV	L,A	
70	MOV	M,B	
71	MOV	M,C	
72	MOV	M,D	
73	MOV	M,E	
74	MOV	M,H	
75	MOV	M,L	
77	MOV	M,A	
78	MOV	A,B	
79	MOV	A,C	
7A	MOV	A,D	
7B	MOV	A,E	
7C	MOV	A,H	
7D	MOV	A,L	
7E	MOV	A,M	
7F	MOV	A,A	

ACCUMULATOR*

80	ADD	B
81	ADD	C
82	ADD	D
83	ADD	E
84	ADD	H
85	ADD	L
86	ADD	M
87	ADD	A
88	ADC	B
89	ADC	C
8A	ADC	D
8B	ADC	E
8C	ADC	H
8D	ADC	L
8E	ADC	M
8F	ADC	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
96	SUB	M
97	SUB	A
98	SBB	B
99	SBB	C
9A	SBB	D
9B	SBB	E
9C	SBB	H
9D	SBB	L
9E	SBB	M
9F	SBB	A
A0	ANA	B
A1	ANA	C
A2	ANA	D
A3	ANA	E
A4	ANA	H
A5	ANA	L
A6	ANA	M
A7	ANA	A
A8	XRA	B
A9	XRA	C
AA	XRA	D
AB	XRA	E
AC	XRA	H
AD	XRA	L
AE	XRA	M
AF	XRA	A
B0	ORA	B
B1	ORA	C
B2	ORA	D
B3	ORA	E
B4	ORA	H
B5	ORA	L
B6	ORA	M
B7	ORA	A
B8	CMP	B
B9	CMP	C
BA	CMP	D
BB	CMP	E
BC	CMP	H
BD	CMP	L
BE	CMP	M
BF	CMP	A

MOVE IMMEDIATE

06	MVI	B, D8
0E	MVI	C, D8
16	MVI	D, D8
1E	MVI	E, D8
26	MVI	H, D8
2E	MVI	L, D8
36	MVI	M, D8
3E	MVI	A, D8

Acc IMMEDIATE*

C6	ADI	D8
CE	ACI	D8
D6	SUI	D8
DE	SBI	D8
E6	ANI	D8
EE	XRI	D8
F6	ORI	D8
FE	CPI	D8

LOAD IMMEDIATE

01	LXI	B, D16
11	LXI	D, D16
21	LXI	H, D16
31	LXI	SP, D16

STACK OPS

C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW*
E3	XTHL	
F9	SPHL	

MOVE

40	MOV	B,B	
41	MOV	B,C	
42	MOV	B,D	
43	MOV	B,E	
44	MOV	B,H	
45	MOV	B,L	
46	MOV	B,M	
47	MOV	B,A	
48	MOV	C,B	
49	MOV	C,C	
4A	MOV	C,D	
4B	MOV	C,E	
4C	MOV	C,H	
4D	MOV	C,L	
4E	MOV	C,M	
4F	MOV	C,A	
50	MOV	D,B	
51	MOV	D,C	
52	MOV	D,D	
53	MOV	D,E	
54	MOV	D,H	
55	MOV	D,L	
56	MOV	D,M	
57	MOV	D,A	

INCREMENT**

04	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
3C	INR	A
03	INX	B
13	INX	D
23	INX	H
33	INX	SP

DECREMENT**

05	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
3D	DCR	A
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP

DOUBLE ADD†

09	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP

LOAD/STORE

0A	LDAX	B
1A	LDAX	D
2A	LHLD	Adr
3A	LDA	Adr
02	STAX	B
12	STAX	D
22	SHLD	Adr
32	STA	Adr

SPECIALS

EB	XCHG	
27	DAA*	
2F	CMA	
37	STC†	
3F	CMC†	

INPUT/OUTPUT

D3	OUT	D8
DB	IN	D8

PSEUDO INSTRUCTION

ORG	Adr	
END		
EQU	D16	
SET	D16	
DS	D16	
DB	D8	[,]
DW	D16	[,]
IF	D16	
ENDIF		
MACRO		( )
ENDM		

CONSTANT DEFINITION

0BDH, 1AH	Hex
105D, 105	Decimal
72O, 72Q	Octal
11011B, 00110B	Binary
'TEST', 'A', 'B'	ASCII

OPERATORS

(,)
*, /, MOD, SHL, SHR
+, -
NOT
AND
OR, XOR

STANDARD SETS

A	SET	7
B	SET	0
C	SET	1
D	SET	2
E	SET	3
H	SET	4
L	SET	5
M	SET	6
SP	SET	6
PSW	SET	6

FLAG BYTE STACK FORMAT

7	6	5	4	3	2	1	0
S	Z	Ø	AC	Ø	P	1	CY

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

* = all Flags (C, Z, S, P, AC) affected

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

† = only CARRY affected

Adr = 16 bit address

** = all Flags except CARRY affected; (exception: INX & DCX affect no Flags)

Appendix B. PROGRAMS FOR LIFT AND PITCH

Address		OP Code	Mnemonic Code	Comment
04	00	3E	MVI,A	Start
	1	FF		
	2	32	STA	
	3		DD	
	04		0B	
	5	D3	OUT 4	
	6	04		
	7	CD	CALL I.C.	Set up initial conditions
	08		60	
	9		06	
	A	3E	MVI,A	Begin to operate
	B	08		
	0C	CD	CALL TEST	
	D		30	
	E		03	
	F	C2	JNZ*	If no, jump to *
	10		OA	
	1		04	
ENT1	2	CD	CALL RESCLK	If yes, reset clock
	3		B0	
	14		03	
ENT2	15	3E	MVI,A	Sample $\overline{y}$
	6	FD		
	7	CD	CALL A/D	
	18		00	
	9		03	
	A	32	STA U_o	
	B		D_7	
	1C		0B	
	D	5F	MOV E.A.	$Z \leftarrow Z^* + b_o y$
	E	16	MVI,D	
	F	00		
04	20	2E	MVI,L	
	1	81		
	2	CD	CALL MUL	
	3		90	
	24		03	
	5	2A	LHLD	
	6		D1	
	7		0B	

Address	OP Code	Mnemonic Code	Comment
04 28	CD	CALL ADD1	
9		58	
A		03	
B	0E	MVI,C	
2C	00		
D	06	MVI,B	
E	07		
F	CD	CALL SUB1	
30		60	
1		03	
2	CD	CALL÷4	
3		90	
34		06	
5	CD	CALL÷4	
6		90	
7		06	
38	22	SHLD	
9		D1	
A		OB	
B	3E	MVI,A	Sample r
3C	FC		
D	CD	CALL A/D	
E		00	
F		03	
40	32	STA	
1		DA	
2		0B	
3	4F	MOV C.A.	e←r-Z(n)
44	06	MVI,B	
5	00		
6	CD	CALL SUB2	
7		F8	
48		03	
9	22	SHLD	
A		DB	
B		0B	
4C	CD	CALL÷4	
D		90	
E		06	
F	CD	CALL÷4	

Address	OP Code	Mnemonic Code	Comment
04 50		90	
1		06	
2	0E	MVI,C	
3	FF		
54	06	MVI,B	
5	00		
6	CD	CALL ADD1	
7		58	
58		03	
9	3E	MVI,A	Output e
A	DF	.	
B	CD	CALL D/A	
5C		C0	
D		02	
E	3E	MVI,A	
F	10		
60	CD	CALL TEST	
1		30	
2		03	
3	2E	MVI L	
64		D7	
5	26	MVI H	
6		0B	
7	CC	CZ PRINT	
68		C0	
9		06	
A	2E	MVI L	Update data
B	D8		
6C	26	MVI H	
D	0B		
E	CD	CALL MOVE	
F		D0	
70		03	
1	CD	CALL $\Sigma\ a_i Z_i$	Calculate Z*
2		A0	
3		04	
74	3A	LDA	
5		DD	
6		0B	
7	E6	ANI	

Address		OP Code	Mnemonic Code	Comment
04	78	FF		
	9	C8	RZ	
	A	3E	MVI A	Hold?
	B	08		
	7C	CD	CALL TEST	
	D		30	
	E		03	If hold, jump **
	F	C2	JNZ**	
	80		7A	
	1		04	
***	2	CD	CALL TIME	Time for next sampling
	3		C0	
	84		03	
	5	DE	SBI	
	6	EA		
	7	FA	JM***	No jump ***
	88		82	
	9		04	
	A	C3	JMP ENT1	Yes, jump ENT1
	B		12	
	8C		04	
	D			
	E			
	F			
	90			
	1			
	2			
	3			
	94			
	5			
	6			
	7			
	98			
	9			
	A			
	B			
	9C			
	D			
	E			
	F			

Address		OP Code	Mnemonic Code	Comment
			Calculate Z*	
04	A0	3A	LDA	$Z^* \leftarrow b_2 U_2$
	1		D9	
	2		0B	
	3	5F	MOV E.A.	
	A4	16	MVI D	
	5	00		
	6	2E	MVI L	
	7	22		
	A8	CD	CALL MUL	
	9		90	
	A		03	
	B	60	MOV H.B.	
	AC	69	MOV L C	
	D	22	SHLD	
	E		D1	
	F		0B	
	B0	2A	LHLD	$Z^* \leftarrow Z^* \leftarrow a_i Z_i$
	1		D3	
	2		0B	
	3	5D	MOV E.L.	
	B4	54	MOV D.H.	
	5	2E	MVI.L	
	6	04	a_1	
	7	CD	CALL MUL	
	B8		90	
	9		03	
	A	2A	LHLD	
	B		D1	
	BC		0B	
	D	CD	CALL SUB1	
	E		60	
	F		03	
	C0	22	SHLD	
	1		D1	
	2		0B	
	3	2A	LHLD	$Z^* \leftarrow Z^* - 0_2 Z_2$
	C4		D5	
	5		0B	
	6	5D	MOV E.L.	
	7	54	MOV D.H.	

Address		OP Code	Mnemonic Code	Comment
04	C8	2E	MVI.L	
	9	03		
	A	CD	CALL MUL a_2	
	B		90	
	CC		03	
	D	2A	LHLD	
	E		D1	
	F		0B	
	D0	CD	CALL SUB1	
	1		60	
	2		03	
	3	22	SHLD	
	D4		D1	
	5		0B	
	6	3A	LDA	$Z^* \; Z^*-b_1U_1$
	7		D8	
	D8		0B	
	9	5F	MOVE.A	
	A	16	MVL.D	
	B	00		
	DC	2E	MVI.L	
	D	8D		
	E	CD	CALL MUL	
	F		90	
	E0	03		
	1	2A	LHLD	
	2		D1	
	3		0B	
	E4	CD	CALL SUB1	
	5		60	
	6		03	
	7	22	SHLD	
	E8		D1	
	9		0B	
	A	C9	RET	
	B			
	EC			
	D			
	E			
	F			

Address		OP Code	Mnemonic Code	Comment
04	F0			
	1			
	2			
	3			
	F4			
	5			
	6			
	7			
	F8			
	9			
	A			
	B			
	FC			
	D			
— —	E	—		
	F			
			Pitch	
05	00	3E	MVI.A	Start
	1	FF		
	2	32	STA	
	3		DD	
	04		0B	
	5	D3	OUT4	
	6	04		
	7	CD	CALL I.C.	Set up initial conditions
	08		60	
	9		06	
	A	3E	MVI.A	Begin to operate
	B	08		
	0C	CD	CALL TEST	
	D		30	
	E		03	
	F	C2	JNZ*	If no, jump *
	10		0A	
	1		05	
ENT1	2	CD	CALL RESCLK	Yes, reset clock
	3		B0	
	14		03	
ENT2	15	3E	MVI.A	Sample y
	6	FF		
	7	CD	CALL A/D	

Address		OP Code	Mnemonic Code	Comment
ENT2	18		00	
	9		03	
	A	32	STAU.	
	B		F7	
	1C		0B	
	D	5F	MOV E.A.	
	E	16	MVI D	$Z \leftarrow Z^* + b_o y$
	F	00		
05	20	2E	MVI.L	
	1	11		
	2	CD	CALL MUL	
	3		90	
	24		03	
	5	2A	LHLD	
	6		F1	
	7		0B	
	28	CD	CALL ADD1	
	9		58	
	A		03	
	B	0E	MVI.C	
	2C	00		
	D	06	MVI.B	
	E	07		
	F	CD	CALL SUB1	
	30		60	
	1		03	
	2	CD	CALL÷4	
	3		90	
	34		06	
	5	CD	CALL÷4	
	6		90	
	7		06	
	38	22	SHLD	
	9		F1	
	A		0B	
	B	3E	MVI.A	Sample r
	3C	FE		
	D	CD	CALL A/D	
	E		00	
	F		03	

Address	OP Code	Mnemonic Code	Comment
05 40	32	STA	
1		FA	
2		0B	
3	4F	MOV C.A.	e r-Z(n)
44	06	MVI.B	
5	00		
6	CD	CALL SUB2	
7		F8	
48		03	
9	22	SHLD	
A		FB	
B		0B	
4C	CD	CALL÷4	
D		90	
E		06	
F	00	NOP	
50	00	NOP	
1	00	NOP	
2	0E	MVI.C	
3	FF		
54	06	MVI.B	
5	00		
6	CD	CALL ADD1	
7		58	
58		03	
9	3E	MVI.A	Output e
A	BF		
B	CD	CALL D/A	
5C		C0	
D		02	
E	3E	MVI.A	
F	10		
60	CD	CALL TEST	
1		30	
2		03	
3	2E	MVI.L	
64	F7		
5	26	MVI.H	
6	0B		
7	CC	CZ PRINT	

Address		OP Code	Mnemonic Code	Comment
05	68		C0	
	9		06	
	A	2E	MVI.L	Update data
	B	F8		
	6C	26	MVI.H	
	D	0B		
	E	CD	CALL MOVE	
	F		D0	
	70		03	
	1	CD	CALL $\Sigma a_i Z_i$	Calculate Z*
	2		A0	
	3		05	
	74	3A	LDA	
	5		DD	
	6		0B	
	7	E6	ANI	
	78	FF		
	9	C8	RZ	
**	A	3E	MVI.A	
	B	08		Hold?
	7C	CD	CALL TEST	
	D		30	
	E		03	
	C	C2	JNZ**	If hold, jump **
	80		7A	
	1		05	
***	2	CD	CALL TIME	Time for next sampling
	3		C0	
	84		03	
	5	DE	SBl	
	6	4E		
	7	FA	JM***	No, jump ***
	88		82	
	9		05	
	A	C3	JMPEND	Yes, jump
	B		12	ENTl
	8C		05	
	D			
	E			
	F			

Address	OP Code	Mnemonic Code	Comment
05 90			
1			
2			
3			
94			
5			
6			
7			
98			
9			
A			
B			
9C			
D			
E			
F			
		Calculate Z*	
05 A0	3A	LDA	$Z^* \leftarrow b_2 U_2$
1		F9	
2		0B	
3	5F	MOV E.A.	
A4	16	MVI.D	
5	00		
6	2E	MVI.L	
7	04		
A8	CD	CALL MUL	
9		90	
A		03	
B	60	MOV H.B.	
AC	69	MOV L.C.	
D	22	SHLD	
E		F1	
F		0B	
B0	2A	LHLD	$Z^* \leftarrow Z^* + a_1 Z_1$
1		F3	
2		0B	
3	5D	MOV E.L.	

Address	OP Code	Mnemonic Code	Comment
05 B4	54	MOV D.H.	
5	2E	MVI.L	
6	0D	a_1	
7	CD	CALL MUL	
B8		90	
9		03	
A	2A	LHLD	
B		F1	
BC		0B	
D	CD	CALL ADD1	
E		58	
F		03	
C0	22	SHLD	
1		F1	
2		0B	
3	2A	LHLD	$Z^* \leftarrow Z^* - a_2 Z_2$
C4		F5	
5		0B	
6	5D	MOV E.L.	
7	54	MOV D.H.	
C8	2E	MVI.L	
9	02		
A	CD	CALL MUL	
B		90	
CC		03	
D	2A	LHLD	
E		F1	
F		0B	
D0	CD	CALL SUB1	
1		60	
2		03	
3	22	SHLD	
D4		F1	
5		0B	
6	3A	LDA	$Z^* \leftarrow Z^* - b_1 U_1$
7		F8	
D8		0B	
9	5F	MOV E.A.	
A	16	MVI.D	
B	00		

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Address		OP Code	Mnemonic Code	Comment
05	DC	2E	MVI.L	
	D	11	b_1	
	E	CD	CALL MUL	
	F		90	
	E0		03	
	1	2A	LHLD	
	2		F1	
	3		0B	
	E4	CD	CALL SUB1	
	5		60	
	6		03	
	7	22	SHLD	
	E8		F1	
	9		0B	
	A	C9	RET	
	B			
	EC			
	D			
	E			
	F			
	F0			
	1			
	2			
	3			
	F4			
	5			
	6			
	7			
	F8			
	9			
	A			
	B			
	FC			
	D			
	E			
	F			

Appendix C. PROGRAM FOR ONE-DIMENSIONAL BALANCE

Address		OP Code	Mnemonic Code	Comment
07	00	3E	MVI,A	Start
	1	FF		
	2	D3	OUT4	
	3	04		
	04	CD	CALL IC3	Set up initial conditions
	5		A0	
	6		07	
	7	3E	MVI,A	Begin to operate?
	08	08		
	9	CD	CALL TEST	
	A	30		
	B	03		
	0C	C2	JNZ*	If no, jump *
	D		07	
	E		07	If yes, reset clock
ENT	F	CD	CALL RESET	
07	10	B0		
	1	03		
	2	3E	MVI,A	Sample y
	3	FD		
	14	CD	CALL AD	
	5	00		
	6	03		
	7	32	STA	
	18		00	
	9		09	
	A	2E	MVI, L	$Z_1 \leftarrow B_o y - Z_1$*
	B	00		
	1C	CD	CALL CAL	
	D		C0	
	E		04	
	F	2E	MVI, L	$Z_2 \leftarrow B_2 Z_1 - Z_2$*
	20	06		
	1	CD	CALL CAL	
	2		C0	
	3		04	
	24	2E	MVI, L	$Z_3 \leftarrow B_4 Z_2 - Z_3$*
	5	OC		
	6	CD	CALL CAL	
	7		C0	

Address		OP Code	Mnemonic Code	Comment
07	28		04	
	9	3E	MVI. A	Sample r
	A	FC		
	B	CD	CALL AD	
	2C	00		
	D	03		
	E	32	STA	
	F		20	
	30		09	
	1	06	MVI, B	$e \leftarrow r\text{-}Z_3(n)$
	2	00		
	3	4F	MOV C.A.	
	34	2A	LHLD	
	5		12	
	6		09	
	7	CD	CALL SUB2	
	38	F8		
	9	03		
	A	22	SHLD	
	B		16	
	3C		09	
	D	3E	MVI, A	Integrator in or not
	E	10		
	F	CD	CALL TEST	
	40	30		
	1	03		
	2	C2	JNZ**	If not, jump **
	3		4A	
	44		07	
	5	2E	MVI, L	If yes, $Z_4 \leftarrow B_7 e + Z_4$*
	6	16		
	7	CD	CALL	
	48		28	
	9		08	
	A	CD	CALL÷4	
	B	90		
	4C	06		
	D	3A	LDA	
	E		13	
	F		08	

Address		OP Code	Mnemonic Code	Comment
07	50	4F	MOV C.A	
	1	3A	LDA	
	2		14	
	3		08	
	54	47	MOV B.A	
	5	CD	CALL ADD1	
	6	58		
	7	03		
	58	3E	MVI.A	Output f
	9	DF		
	A	CD	CALL DA	
	B	C0		
	5C	02		
	D	CD	CALL RELOCATE	Update data
	E		80	
	F	05		
	60	2E	MVI.L	Calculate Z_1*
	1	03		
	2	CD	CALL SUM	
	3		20	
	64		05	
	5	2E	MVI.L	Calculate Z_2*
	6	09		
	7	CD	CALL SUM	
	68		20	
	9		05	
	A	2E	MVI,L	Calculate Z_3*
	B	OF		
	6C	CD	CALL SUM	
	D		20	
	E		05	
	F	2E	MVI,L	Calculate Z_4*
	70	19		
	1	CD	CALL SUM	
	2	20		
	3	05		
***1	74	3E	MVI,A	Hold or not?
	5	08		
	6	CD	CALL TEST	
	7	30		

Address		OP Code	Mnemonic Code	Comment
***1	78	03		
	9	C2	JNZ***	If yes, jump ***
	A		74	
	B		07	
	7C	3A	LDA	
	D		12	
	E		08	
	F	47	MOV B.A.	
07+	80	CD	CALL TIME	Check Time
	1	C0		
	2	03		
	3	90	SUB B	
	84	FA	JM+	
	5		80	
	6		07	
	7	C3	JMP ENT	Jump ENT
	88		OF	
	9		07	
	A			
	B			
	8C			
	D			
	E			
	F			
07	90			
	1			
	2			
	3			
	94			
	5			
	6			
	7			
	98			
	9			
	A			
	B			
	9C			
	D			
	E			
	F			
	0			
	1			
	2			
	3			

Address		OP Code	Mnemonic Code	Comment
07	4			
	5			
	6			
	7			
	8			
	9			
	A			
	B			
	C			
	D			
	E			
	F			
	0			
	1			
	2			
	3			
	4			
	5			
	6			
	7			
	8			
	9			
	A			
	B			
	C			
	D			
	E			
	F			

Memory layout of coefficients

08	00	B_o	
	1	B_1	
	2	A_1	
	3	C_{1L}	
	04		
	5	C_{1H}	00
	6	B_2	
	7	B_3	
	08	A_2	
	9	C_{2L}	
	A	C_{2H}	
	B		00

Address	OP Code	Mnemonic Code	Comment
08 0C		B_4	
D		B_5	
E		A_3	
F		C_{3L}	
10		C_{3H}	
1			00
2		TIME	
3		$ADIC_L$	
14		$ADIC_H$	
5			00
6		B_6	41
7		B_7	3F
18		A_4	40
9		C_{4L}	00
A		C_{4H}	00
B			00
1C		ADDSUB 1	
D		2	
E		3	
F		4	00
20		IC_{1L}, e_a	
1		IC_{1H}, e_{CH}	
2		IC_{2L}	
3		IC_{2H}	
24		IC_{3L}	
5		IC_{3H}	
6		IC_{4L}	
7		IC_{4H}	
28	CD	CALL	CD
9		C0	C0
A		05	05
B	C9	RET	C9
2C			
D			
E			
F			
0			
1			
2			
3			

Address		OP Code	Mnemonic Code	omment
08	4			
	5			
	6			
	7			
	8			
	9			
	A			
	B			
	C			
	D			
	E			
	F			

Memory layout of variables

09	00	U(n)
	1	0
	2	U(n-1)
	3	0
	04	Z_{1SL}
	5	Z_{1SH}
	6	$Z_{1(n)L}$
	7	$Z_{1(n)4}$
	08	$Z_{1(n-1)L}$
	9	$Z_{1(n-1)H}$
	A	Z_{2SL}
	B	Z_{2SH}
	0C	$Z_{2(n)L}$
	D	$Z_{2(n)H}$
	E	$Z_{2(n01)L}$
	F	$Z_{2(n-1)H}$
	10	Z_{3SL}
	1	Z_{3SH}
	2	$Z_{3(n)L}$
	3	$Z_{3(n)H}$
	14	$Z_{3(n-1)L}$
	5	$Z_{3(n-1)H}$
	6	$e_{(n)L}$
	7	$e_{(n)H}$
	18	$e_{(n-1)L}$
	9	$e_{(n-1)H}$
	A	Z_{4SL}
	B	Z_{4SH}

Address	OP Code	Mnemonic Code	Comment
09 1C		$Z_{4(n)L}$	
D		$Z_{4(n)H}$	
E		$Z_{4(n-1)L}$	
F		$Z_{4(n-1)H}$	
20		X1	
1			
2			
3			
24			
5			
6			
7			
28			
9			
A			
B			
2C			
D			
E			
F			
30			
1			
2			
3			
34			
5			
6			
7			
38			
9			
A			
B			
3C			
D			
E			
F			

Appendix D. BASIC PROGRAM FOR HYBRID SIMULATION

```
HSPJ     J5-DFC-/7  BASIC/CAPS  V0J-01

10 REM HYBRID SIMULATION PROGRAM  L
20 REM JANUARY 21,1977
30 PRINT "ENTER NO. OF ZEROS"
40 INPUT N
50 PRINT
60 FOR I=1 TO N
70 PRINT "LIST ZERO, ONE AT A TIME"
80 INPUT A(I),B(I)
90 NEXT I
100 PRINT
110 LET M=N
120 GOSUB 1200
130 FOR I=0 TO N
140 LET D(I)=C(I)
145 NEXT I
150 K2=K1
155 PRINT "ENTER NO. OF POLES"
160 INPUT M
165 PRINT
170 FOR I=1 TO M
180 PRINT "LIST POLE, ONE AT A TIME"
185 INPUT A(I),B(I)
190 NEXT I
195 PRINT
200 GOSUB 1200
205 K=K1/K2
210 PRINT "ENTER ORIGINAL SAMPLE PERIOD, SLOW DOWN FACTOR"
215 INPUT T,S
220 PRINT
225 T1=T*S*60
235 FOR I=1 TO M
240 U(I)=0
245 Z(I)=0
250 NEXT I
255 E(1)=0
260 F(1)=0
265 FOR I=1 TO M
270 A(I)=C(I)
280 NEXT I
290 FOR I=0 TO N
300 B(M-N+I)=D(I)*K
310 NEXT I
320 PRINT "NEED DIFFERENCE EQUATION OR NOT?"
325 INPUT J
330 PRINT
335 IF J=0 GO TO 440
350 PRINT "THE DIFFERENCE EQUATION IS "
360 PRINT "Z(N)=  "
370 FOR I=1 TO M
380 PRINT A(I);"Z(N-";I;")+",
390 NEXT I
410 FOR I=M-N TO M-1
```

```
420 PRINT B(I)$"U(N-"$I$")+",
425 NEXT I
430 PRINT B(M)$"U(N-"$M$")"
435 PRINT
440 PRINT "ENTER INTEGRATOR GAIN"
445 INPUT K
450 PRINT
455 C0=K*T/2+1
460 C1=K*T/2-1
465 AOUT(1, ,65)
470 Z(0)=0
475 F(0)=0
480 PRINT "READY TO OPERATE NOW"
485 AINP(3,H)
490 IF H =2 GO TO 500
495 GO TO 485
500 TIMR
505 AINP(1,X1)
510 AINP(2,X2)
515 AOUT(2,1)
520 U(0)=X2
525 Z(0)=Z(0)+B(M-N)*U(M-N)
530 E(0)=X1-Z(0)
540 F(0)=F(0)+C0*E(0)
550 X=F(0)- ,67
560 AOUT(1,X)
570 AOUT(2,0)
580 FOR I=1 TO M
585 Z(M-I+1)=Z(M-I)
590 U(M-I+1)=U(M-I)
595 NEXT I
600 U(1)=F(0)
605 F(1)=F(0)
610 Z(0)=0
615 FOR I=1 TO M
620 Z(0)=Z(0)+A(I)*Z(I)
625 NEXT I
630 FOR I=M-N+1 TO M
635 Z(0)=Z(0)+B(I)*U(I)
640 NEXT I
650 F(0)=F(1)+C1*E(1)
660 AINP(3,H)
670 IF H =2 GO TO 700
680 GO TO 660
700 TIMR(W)
800 IF W =1 GO TO 700
820 GO TO 500
830 STOP
1200 REM  GET DIFFERENCE EQUATION
1205 C(0)=1
1210 C(1)=0
1220 FOR I=1 TO M
1230 C(I)=F(I)-A(I)
1240 NEXT I
```

ORIGINAL PAGE IS
OF POOR QUALITY

```
1245 IF M-1=0 GO TO 1600
1250 C(2)=0
1260 FOR I=1 TO M-1
1270 FOR J=I+1 TO M
1280 C(2)=C(2)+A(I)*A(J)-B(I)*B(J)
1290 NEXT J
1300 NEXT I
1310 IF M-2=0 GO TO 1600
1320 C(3)=0
1330 FOR I=1 TO M-2
1340 FOR J=I+1 TO M-1
1350 FOR I1=J+1 TO M
1360 C(3)=C(3)-A(I)*A(J)*A(I1)+B(I)*B(J)*A(I1)
1362 C(3)=C(3)+A(I)*B(J)*B(I1)+B(I)*A(J)*B(I1)
1370 NEXT I1
1380 NEXT J
1390 NEXT I
1400 IF M-3=0 GO TO 1600
1410 C(4)=0
1420 FOR I=1 TO M-3
1430 FOR J=I+1 TO M-2
1440 FOR I1=J+1 TO M-1
1450 FOR J1=I1+1 TO M
1460 C(4)=C(4)+A(I)*A(J)*A(I1)*A(J1)-B(I)*B(J)*A(I1)*A(J1)
1461 C(4)=C(4)-A(I)*B(J)*B(I1)*A(J1)-B(I)*A(J)*B(I1)*A(J1)
1462 C(4)=C(4)-A(I)*A(J)*B(I1)*B(J1)+B(I)*B(J)*B(I1)*B(J1)
1463 C(4)=C(4)-A(I)*B(J)*A(I1)*B(J1)-B(I)*A(J)*A(I1)*B(J1)
1470 NEXT J1
1480 NEXT I1
1490 NEXT J
1500 NEXT I
1510 IF M-4=0 GO TO 1600
1520 C(5)=-A(1)*A(2)*A(3)*A(4)*A(5)+B(1)*B(2)*A(3)*A(4)*A(5)
1521 C(5)=C(5)+A(1)*B(2)*B(3)*A(4)*A(5)
1522 C(5)=C(5)+B(1)*A(2)*B(3)*A(4)*A(5)
1523 C(5)=C(5)+A(1)*A(2)*B(3)*B(4)*A(5)
1529 C(5)=C(5)-B(1)*B(2)*B(3)*B(4)*A(5)
1535 C(5)=C(5)+A(1)*B(2)*A(3)*B(4)*A(5)
1540 C(5)=C(5)+B(1)*A(2)*A(3)*B(4)*A(5)
1600 K1=0
1610 FOR I=0 TO M
1620 K1=K1+C(I)
1640 NEXT I
1650 RETURN
1700 END

READY
```

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15 Supplementary Notes

16. Abstract

The feasibility of using a digital computer for performing the automatic control functions for a magnetic suspension and balance system for use with wind tunnel models is investigated. Modeling is done using both the NASA-MIT prototype MSBS and a one-dimensional magnetic balance. A microcomputer using the Intel 8080 Microprocessor is described and results are given using this microprocessor to control the one-dimensional balance.

Hybrid simulations for one degree of freedom of the MSBS were also performed and are reported. It is concluded that use of a digital computer to control the MSBS is eminently feasible and should extend both the accuracy and utility of the system.

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